ADV DIGITAL DESIGN INTRODUCTION

Lecture 1

Dr. Shoab A. Khan

Outline

- Introduction
- Advancement in VLSI Technology
- Computationally Intensive Signal Processing Application
- FPGAs Technology
- CARE VLSI Profile & Achievements
- Design Examples
- Conclusion

Course Information

- Prerequisites:
  - Logic Design,
  - Computer Architecture/Organization
  - Signals and Systems/ Digital Signal Processing

- Text Book
  - Digital Design of Signal Processing System by Shoab Khan Feb 2011, John Wiley & Sons

- Website
  - www.drshoabkhan.com

- References
  - Verilog HDL-A guide to digital design and synthesis by Samir Palnitkar
  - Advanced Digital Design With Verilog HDL by Ciletti, Michael D.

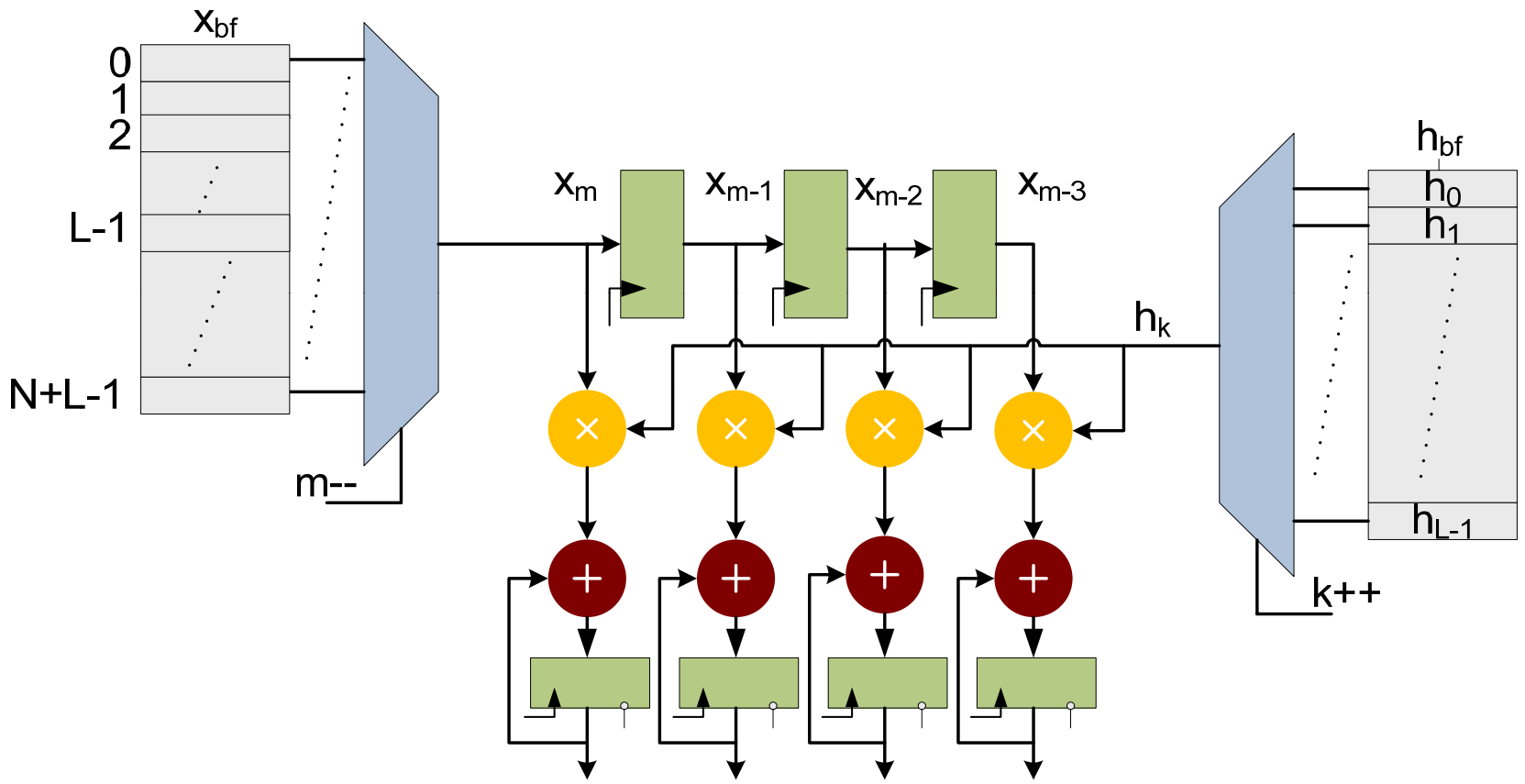
Introduction

- Digital Design means
  - Mapping algorithms/applications in silicon
  - Applying transformations and tricks that results in optimal mapping in competing design space of
    - Area
    - Power dissipation
    - Performance
    - Testabliity
- VLSI has enabled solutions to intractable engineering problems
- Rapid advancement has led to new dimensions in the technology
  - VLSI has revolutionized the commercial market

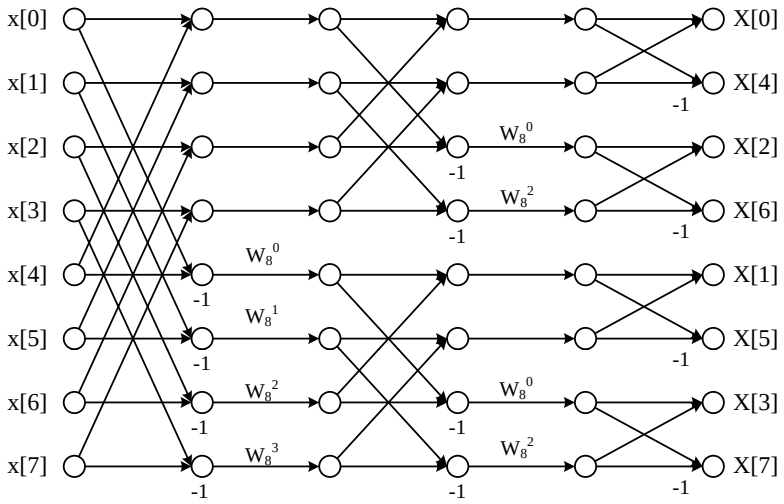
Algorithm implemented in C

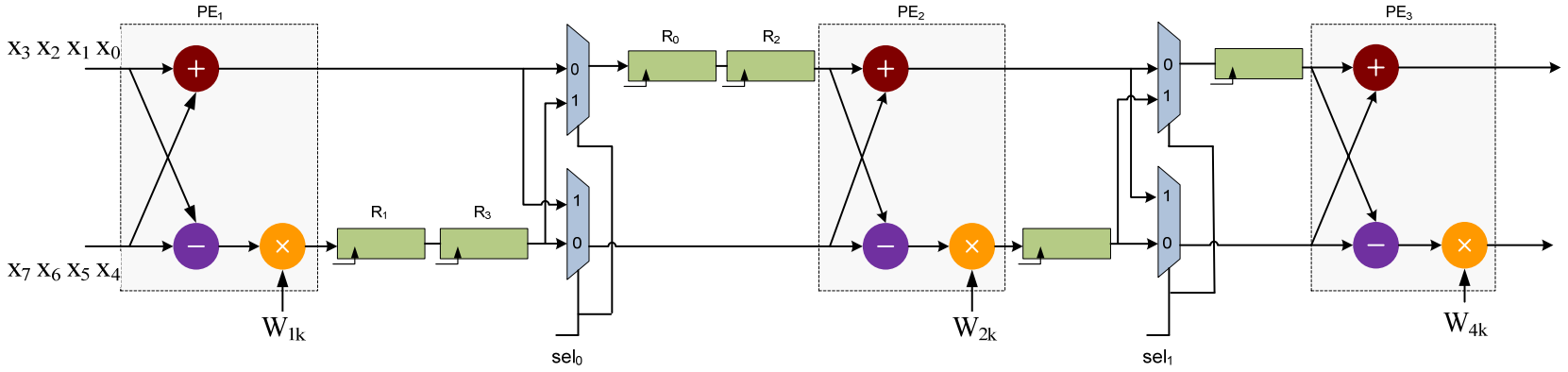
```
#include <stdio.h >
#define N 12
#define L 8
// Test data and filter coefficients
short xbf[N+L-1]={1, 1, 2, 3, 4, 1, 2, 3, 1, 2, 1, 4, 5, -1, 2, 0, 1, -2, 3};
short hbf[L]={5, 9, -22, 11, 8, 21, 64, 18};
short ybf[N];
// The function performs block filtering operation
void BlkFilter(short *xptr, short *hptr, int len_x, int len_h, short *ybf)
{
    int n, k, m;
    for (n=0; n<len_x; n++)
    {
        sum = 0;
        for(k=0, m=n; k<len_h; k++, m--)
            sum += xptr[m]*hptr[k]; // MAC operation
        ybf[n] = sum;
    }
}
// Program to test BlkFilter and BlkFilterUnroll functions
void main(void)
{
    short *xptr, *hptr;
    xptr = &xbf[L-1]; // xbf has L-1 old samples
    hptr = hbf;
    BlkFilterUnroll (xptr, hptr, N, L, ybf);
    BlkFilter (xptr, hptr, N, L, ybf);
}
```

HW mapping of the code in previous slide

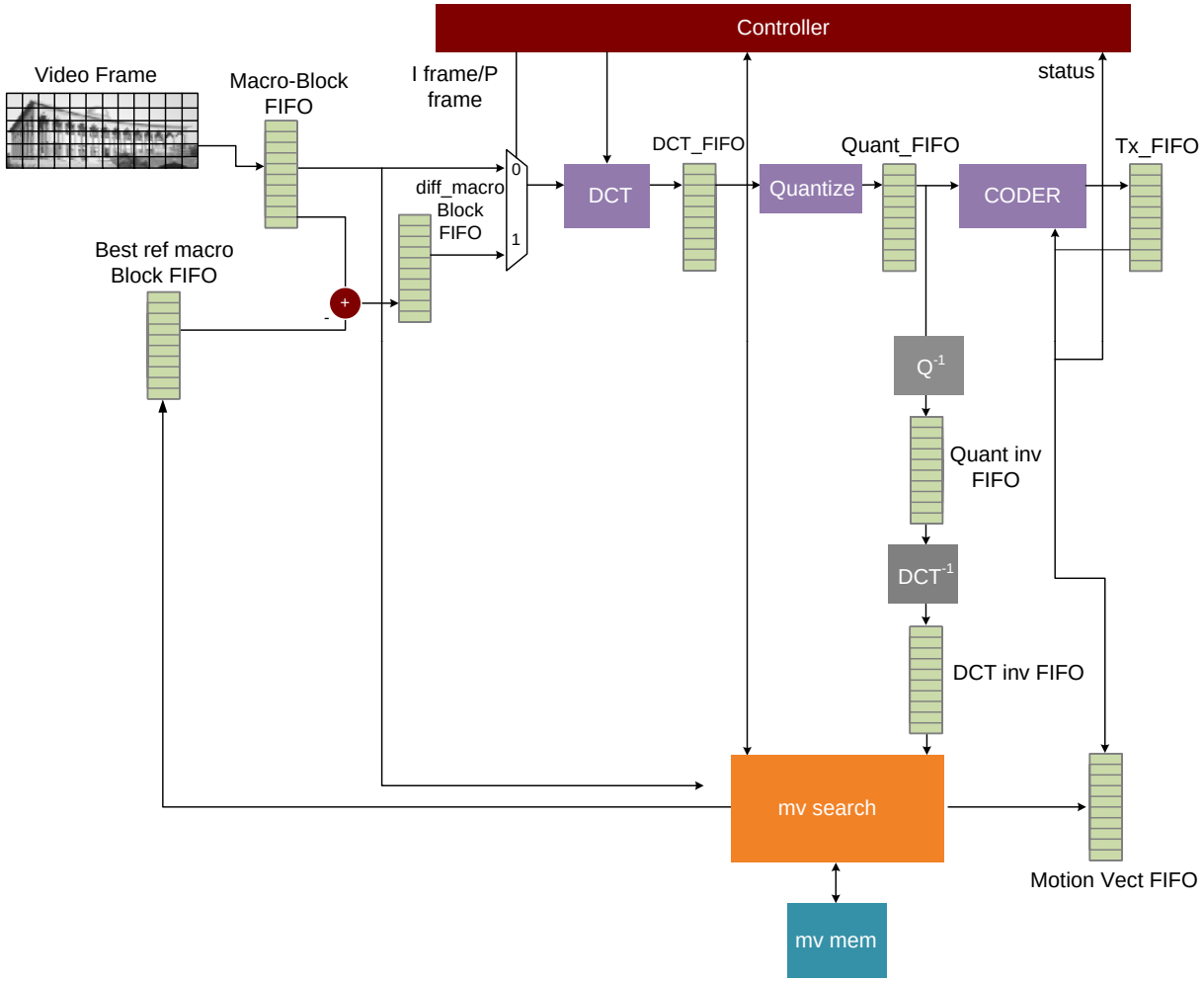


FFT Algorithm & mapping





MPEG Top Level Architecture



Course Outline

- High-level digital design methodology using Verilog, Design, Implementation, and Verification.
- Introduction of SystemVerilog and SystemC
- Application requiring HW implementation, Floating-Point to Fixed-Point Conversion
- Options for top-level design
  - KPN based design
  - Network on Chip
- FPGA Architectures:
  - Embedded Blocks, Multipliers, Adders, Carry Chains
  - Embedded Processors, and interfaces
  - System generator
  - Logic Synthesis
- Architectures for Basic Building Blocks, Adder, Compression Trees, and Multipliers, Barrel Shifter
- Dedicated Fully Parallel Architecture
- Transformations for high speed
  - Unfolding
  - Pipelining
  - Retiming
  - Look-ahead transformation
  - C-Slow
  - Parallel processing
- Optimized Time shared Architecture
  - Folding transformation
- Hardwired State Machine based Design
- Micro Program State Machine based Design

Advancement in VLSI

- The advancement and growth in VLSI has been exponential
- An interesting comment by Bill Gates

"If GM had kept up with the technology like the computer industry has, we would all be driving $25.00 cars that got 1,000 miles to the gallon."

In response to Bill's comments, General Motors issued a press release stating:

If GM had developed technology like Microsoft, we would all be driving cars with the following characteristics:

1. For no reason at all, your car would crash twice a day.

2. Every time they repainted the lines on the road, you would have to buy a new car.

3. Occasionally, executing a maneuver such as a left-turn would cause your car to shut down and refuse to restart, and you would have to reinstall the engine.

4. When your car died on the freeway for no reason, you would just accept this, restart and drive on.

5. Only one person at a time could use the car, unless you bought 'Car95' or 'CarNT', and then added more seats.

In response to Bill's comments, General Motors issued a press release stating:

6. Apple would make a car powered by the sun, reliable, five times as fast, and twice as easy to drive, but would run on only five per cent of the roads.

7. Oil, water temperature and alternator warning lights would be replaced by a single 'general car default' warning light.

8. New seats would force every-one to have the same size butt.

9. The airbag would say 'Are you sure?' before going off.

10. Occasionally, for no reason, your car would lock you out and refuse to let you in until you simultaneously lifted the door handle, turned the key, and grabbed the radio antenna.

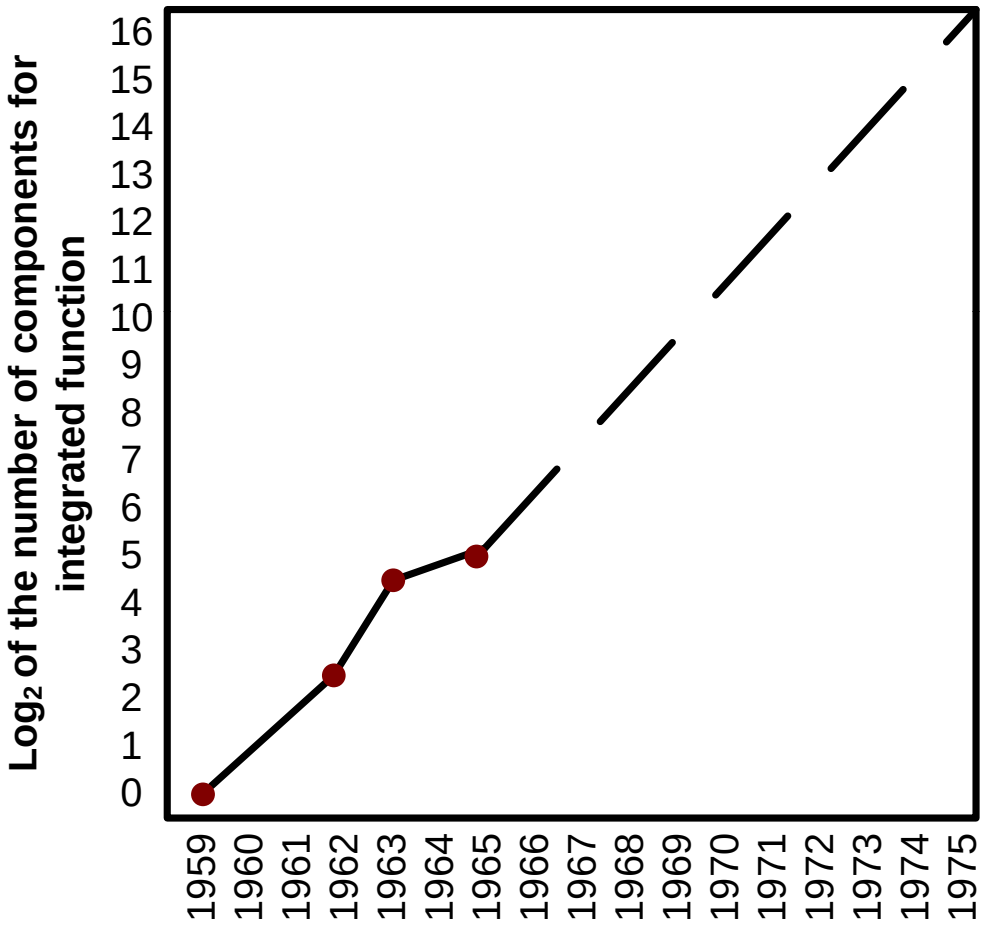
11. Every time GM introduced a new model, car buyers would have to learn how to drive all over again because none of the controls would operate in the same manner as the old car.

12. You would press the 'start' button to shut off the engine.

Fueling the Innovation: Moore's Law

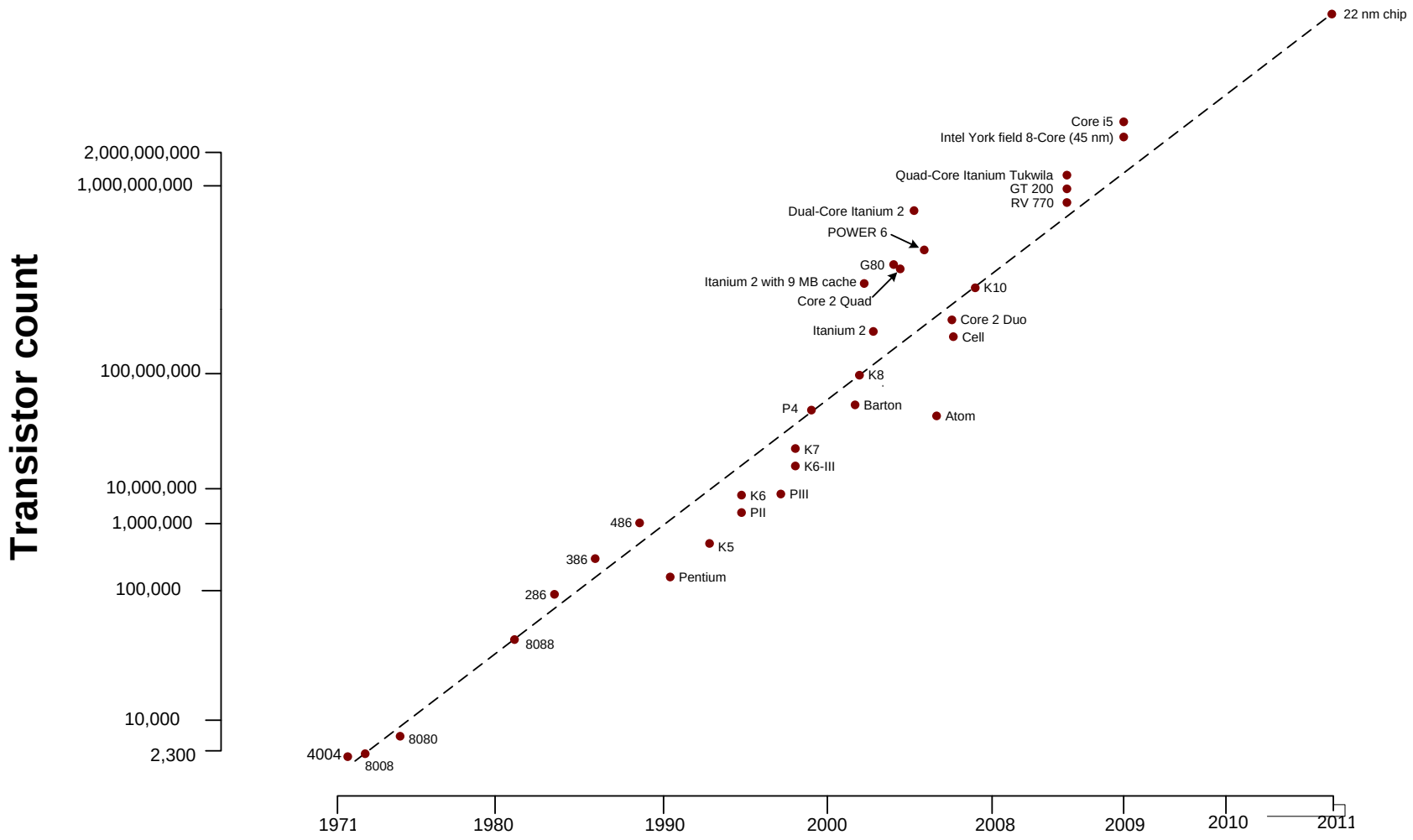
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law



Electronics, April 19, 1965.

Intel continues to pursue Moore's Law

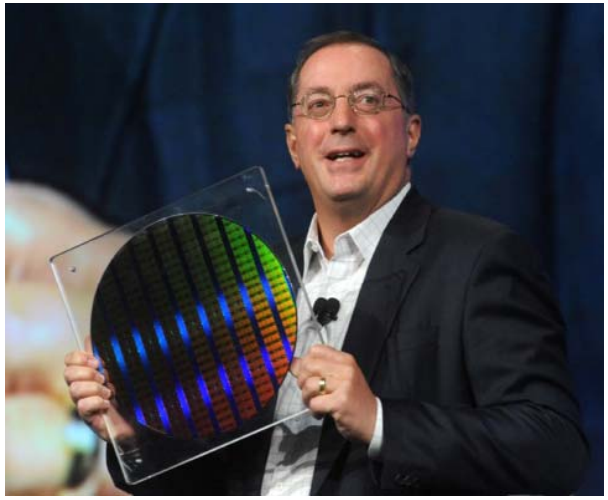


Moore's Plenary Address at ISSCC 2003

NO EXPONENTIAL IS FOREVER . . .
BUT
WE CAN DELAY
"FOREVER"

2.9 billion transistor Chip: Intel still riding on Moore's Curve

Year	Nanometers (nm)	Micrometers (Âµm)
1957	120,000	120.0
1963	30,000	30.0
1971	10,000	10.0
1974	6,000	6.0
1976	3,000	3.0
1982	1,500	1.5
1985	1,300	1.3
1989	1,000	1.0
1993	600	0.6
1996	350	0.35
1998	250	0.25
1999	180	0.18
2001	130	0.13
2003	90	0.09
2005	65	0.065
2008	45	0.045
2009	32	0.032
2011	22	0.022



- 22 Sep 2009, Intel President and CEO Paul Otellini showing a silicon wafer containing the first working chips built on 22nm technology

Where Intel is Today?

- Intel plans to release chips based on a 22 nanometer process technology in the second half of 2011
- The 22nm chip integrates more than 2.9 billion transistors into an area the size of a fingernail
- This doubles the density of the current 32nm chips
- Most of Intel's CPUs today are based on 45nm process
- By comparison, the Intel 4004 microprocessor released in 1971 was based on 10,000nm process.

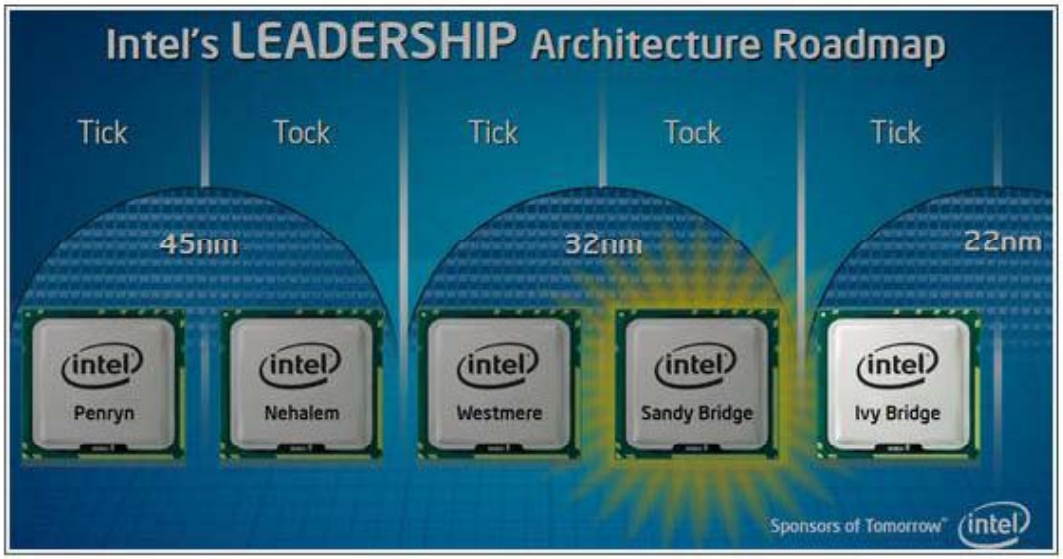
  (A human hair is approximately 100,000 nanometers)

Roadmap confirms 22nm Ivy Bridge in March-April 2012

CPU / Chipset | 2011/05/26 11:19 | Jacob Hugosson | E-mail | Print | Comments (0)

We reported earlier that Intel has postponed the launch of Ivy Bridge to March-April 2012 and a leaked roadmap from Intel confirms this. There are several possible reasons behind this, but it is most likely a market strategy from Intel.

This may have come a bit unexpected for Intel to move Ivy Bridge to a later date than we are accustomed to with the Tick-Tock strategy, but there are most likely good reasons for this.



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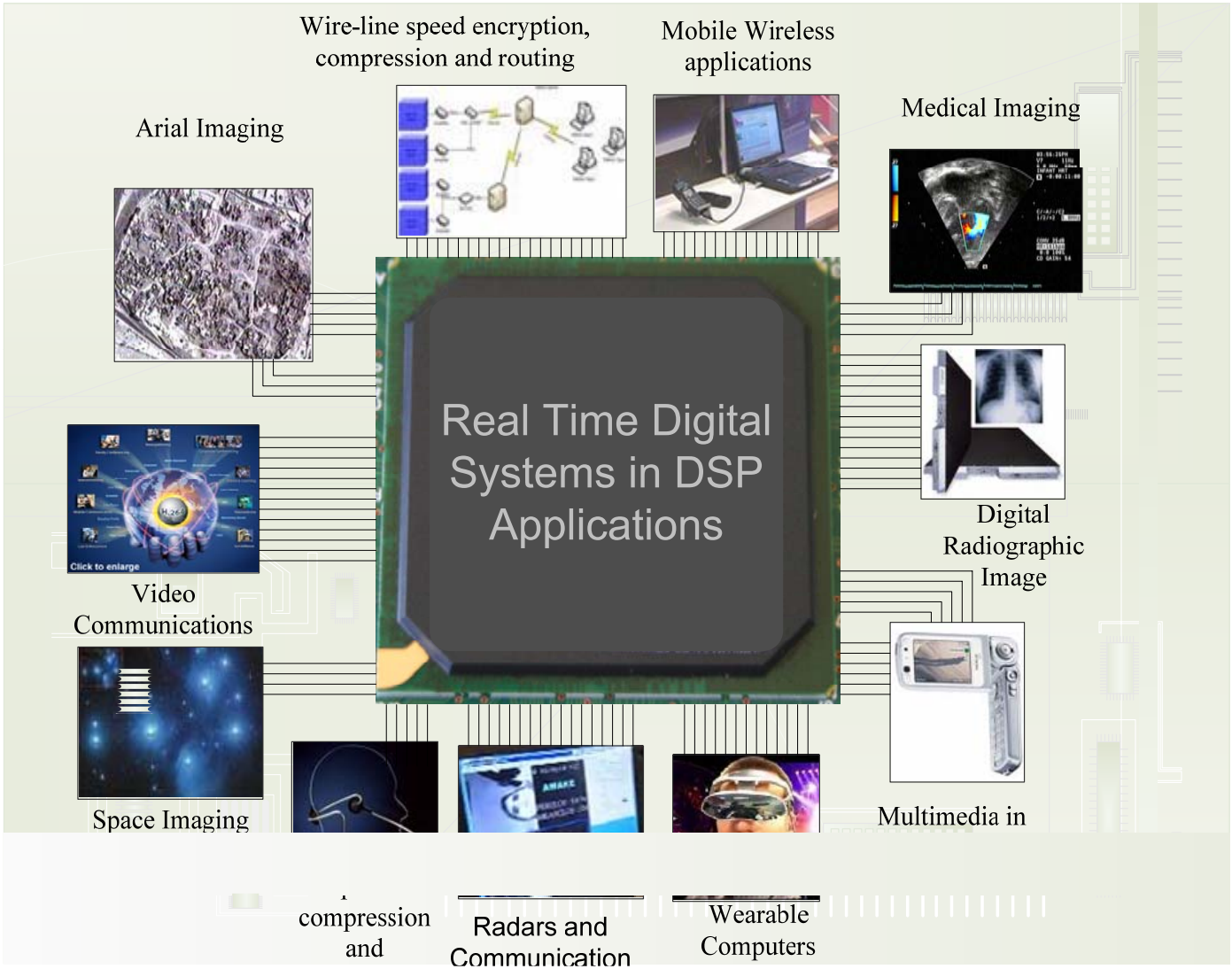
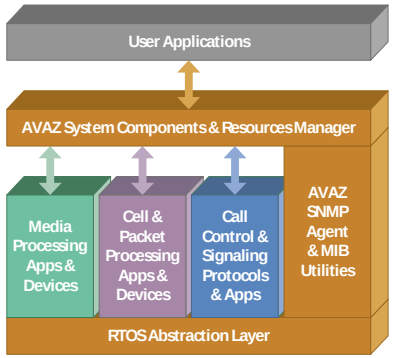
Digital Systems in DSP Applications



VLSI Profile

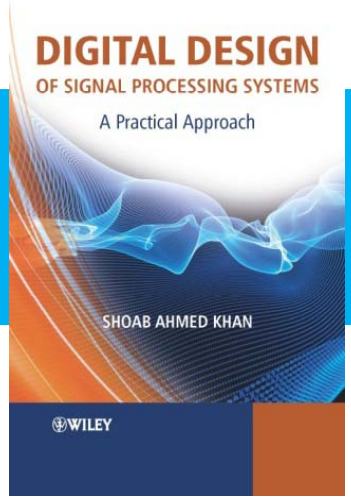


Delivered seven first-time right ASICs/Solutions to NEC, Scientific Atlanta, Nortel Networks, STM Wireless

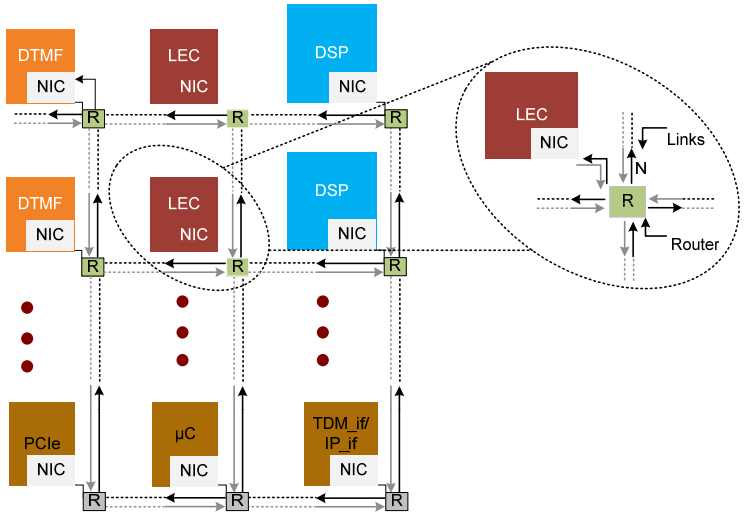
World Highest Density Media Processing Chip Developed in Pakistan in 2000

Developed world highest density media processor chip

Hold patents on multiprocessor based SoC design



Example: SoC for Carrier-class VoIP Media Gateway



- Carrier Class VoIP Media gate performs on thousands of voice channels
  - DTMF detection and generation
  - Line Echo Cancellation
  - Voice compression and decompression
- Multiple layers of application-specific PEs are linked with an NoC for inter-processor communication

My views few years back

- “I consider FPGA as the most exciting invention of electronics after transistor. It is an amazing device, that can take any configuration as per the designer’s desires. The technology is of special interest to engineers in developing countries as it enables them to design and implement multi million gates logic. They can realize astonishing solution to mathematically intractable problems. “


10th INTERNATIONAL APICTA 2010 AWARDS
MERIT
Best of Communications
Center for Advanced Research in Engineering (CARE)
Software Defined Radio
10th INTERNATIONAL APICTA Awards 2010
October 15th, 2010
YBhg Tan Sri Abdul Halim Ali
Mr. Sutee Satanasathapon
MDEC


10th INTERNATIONAL APICTA 2010 AWARDS
MERIT
Best of Security Applications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Center for Advanced Research in Engineering (CARE)
Digital Radio Surveillance Equipment
10th INTERNATIONAL APICTA Awards 2010
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YBhg Tan Sri Abdul Halim Ali
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CARE does Pakistan proud at APICTA 2010
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APICTA 2010
The team from the Center for Advanced Research in Engineering (CARE) swept the Silver at the Asia Pacific ICT Awards (APICTA) in Kuala Lumpur on October 15, 2010
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@kidvai thanks. Will assess the situation tomorrow.
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GOLD SPO
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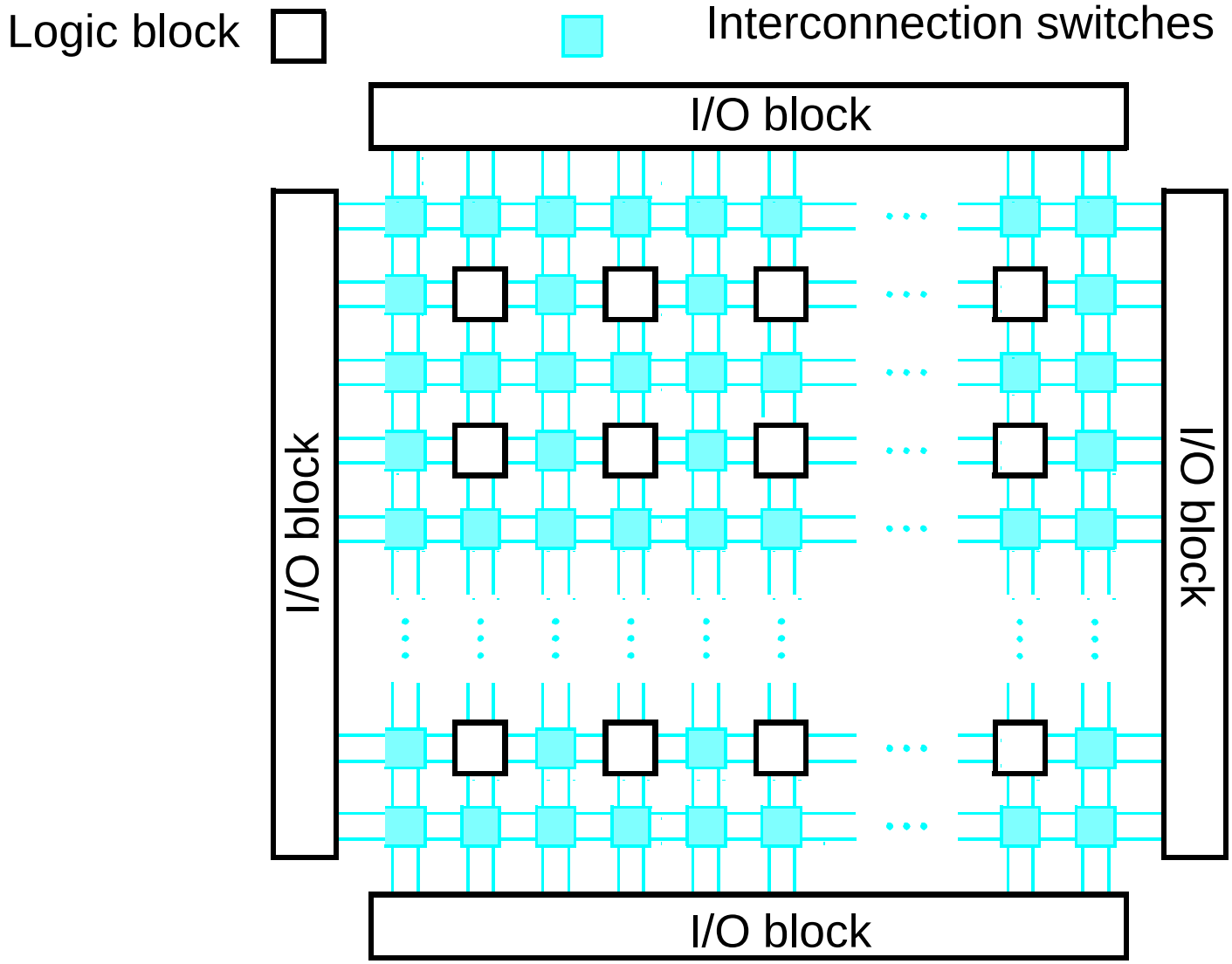
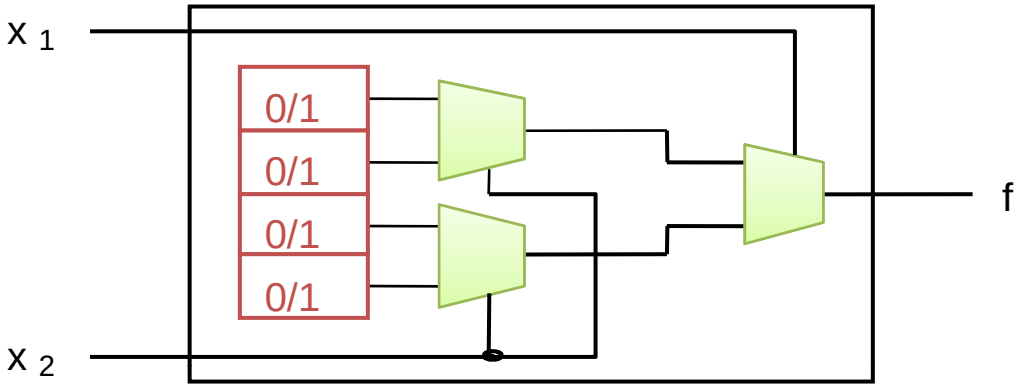


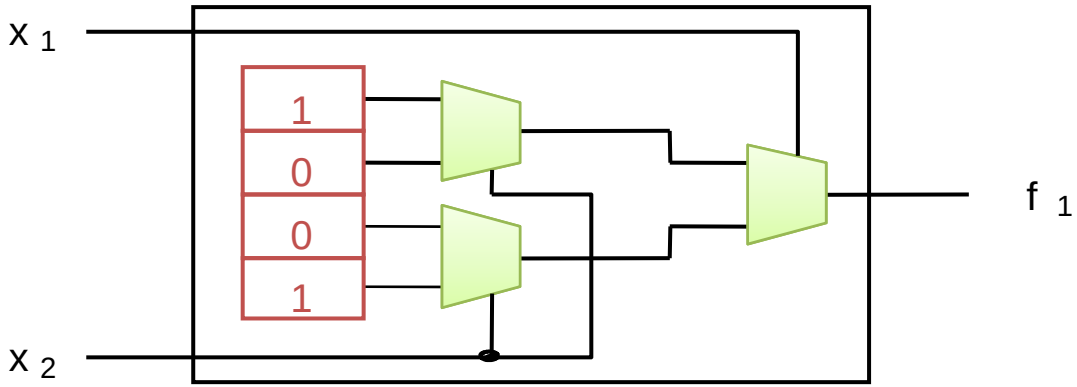
Structure of an FPGA



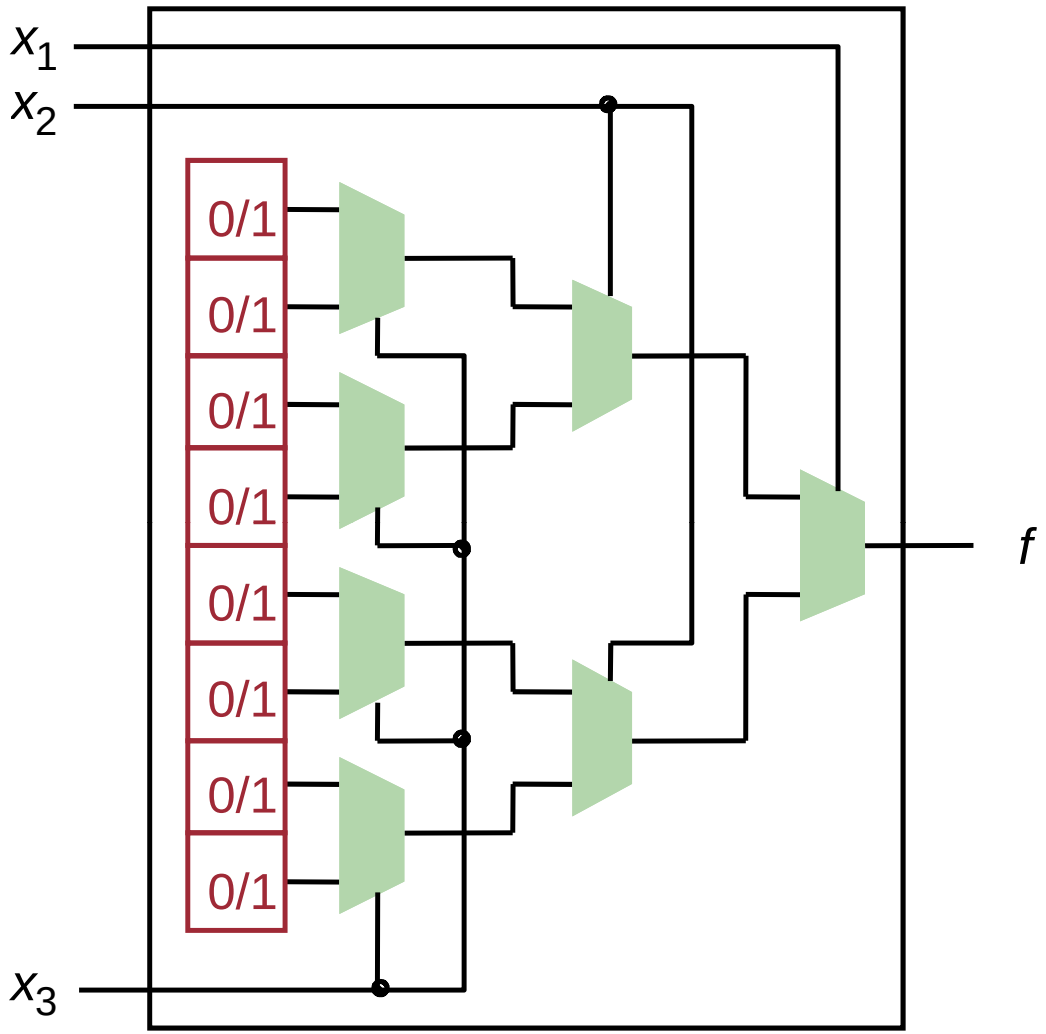
(a) Circuit for a two-input LUT

x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1

(b) $f_1 = \bar{x}_1 \bar{x}_2 + x_1 x_2$

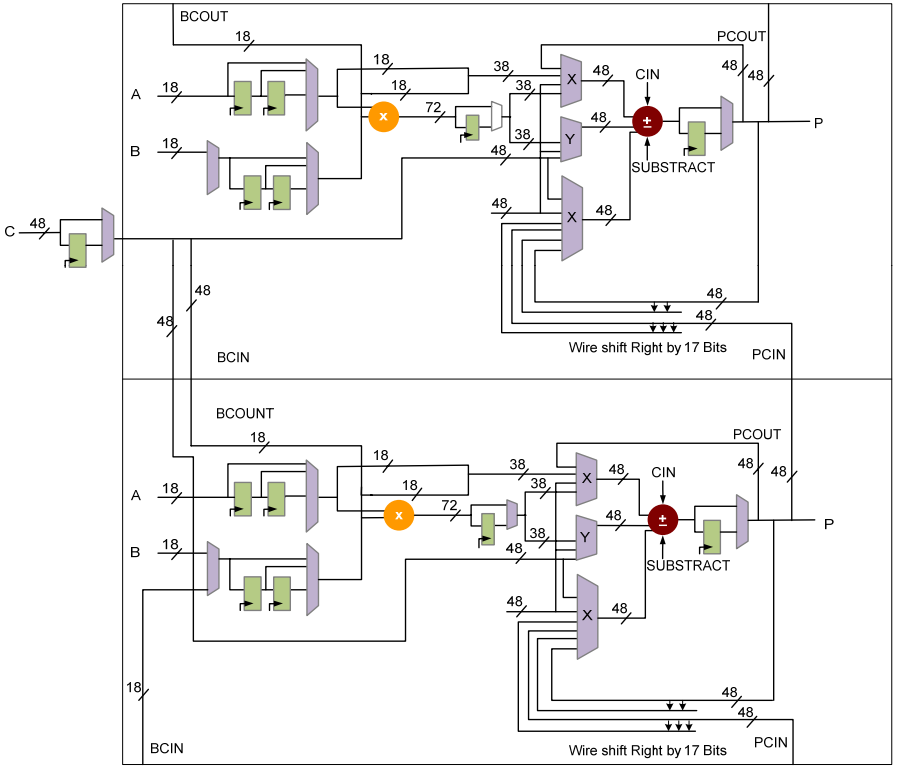


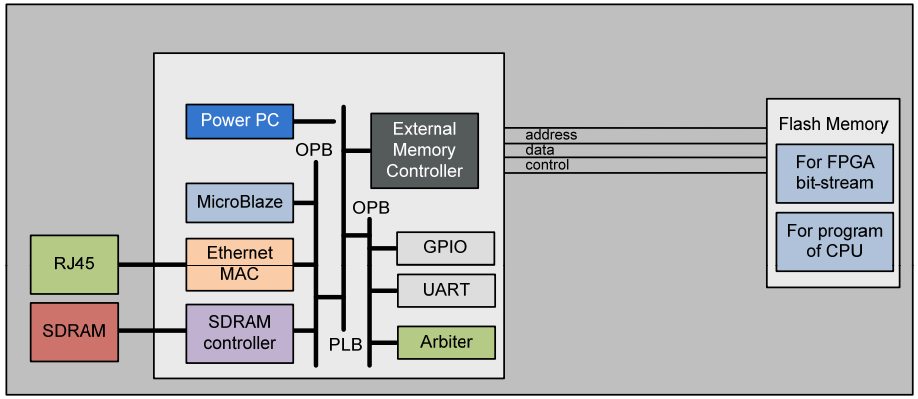
(c) Storage cell contents in the LUT



A three-input LUT

FPGAs Embedding Elements

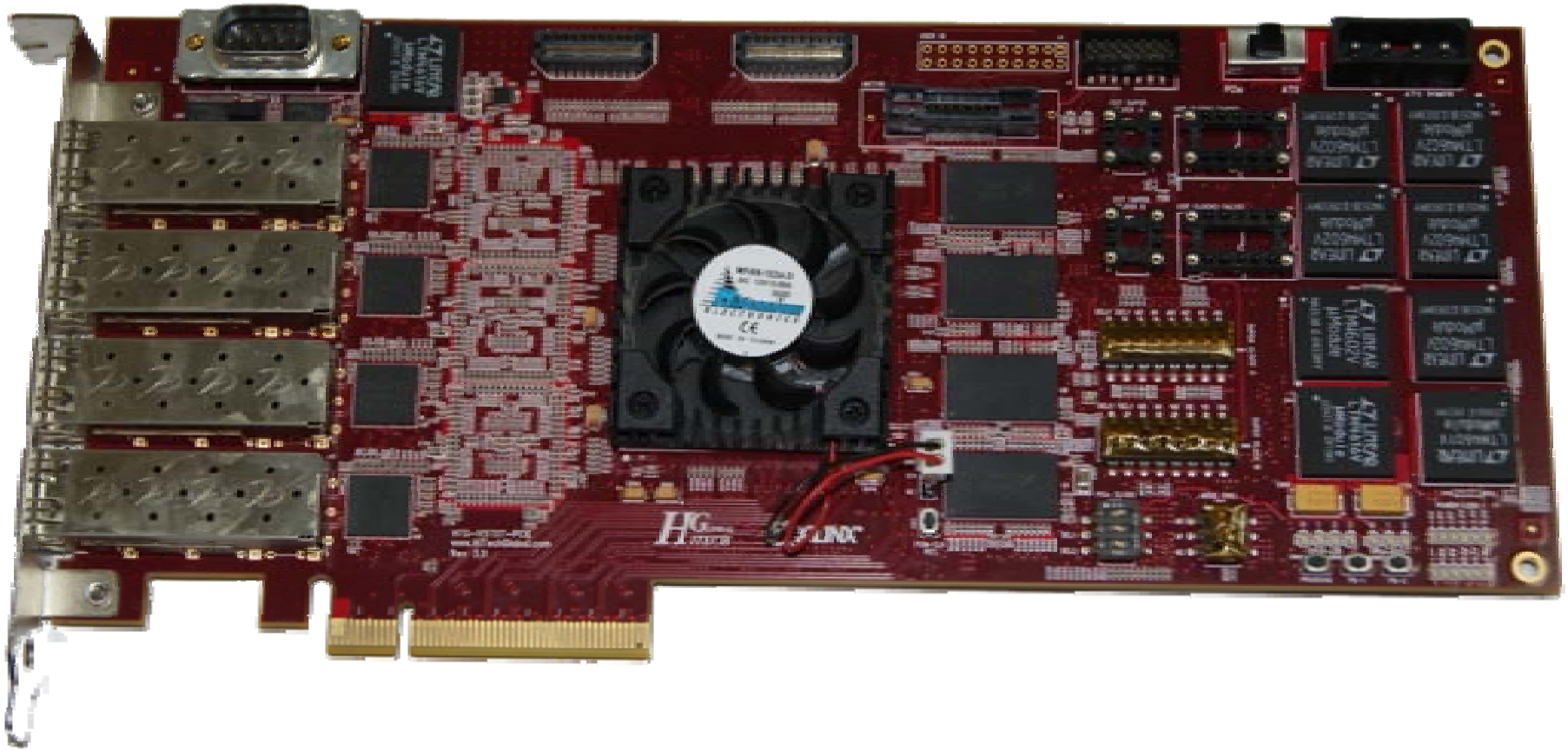




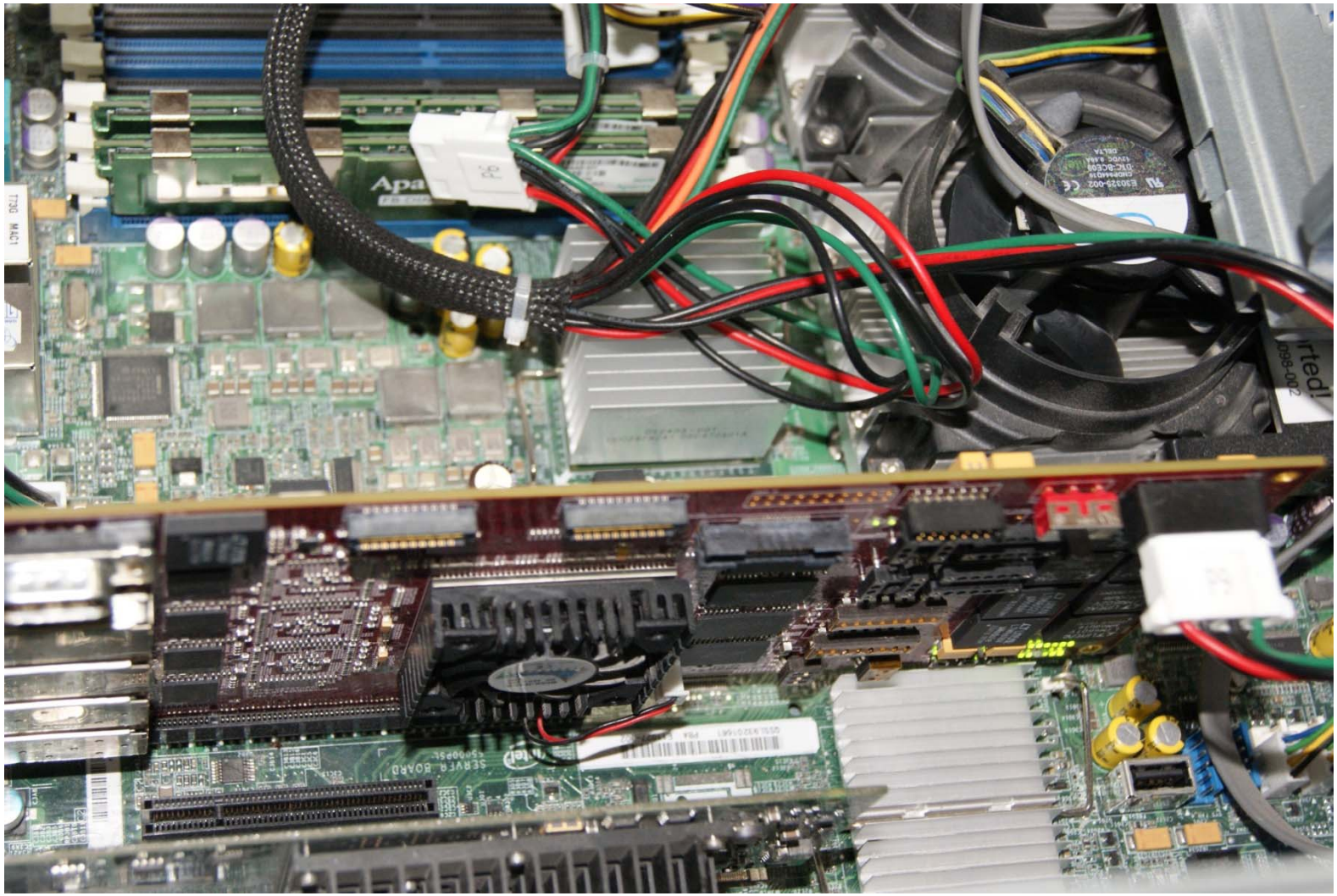
Design Examples

10 GB Network Analysis System

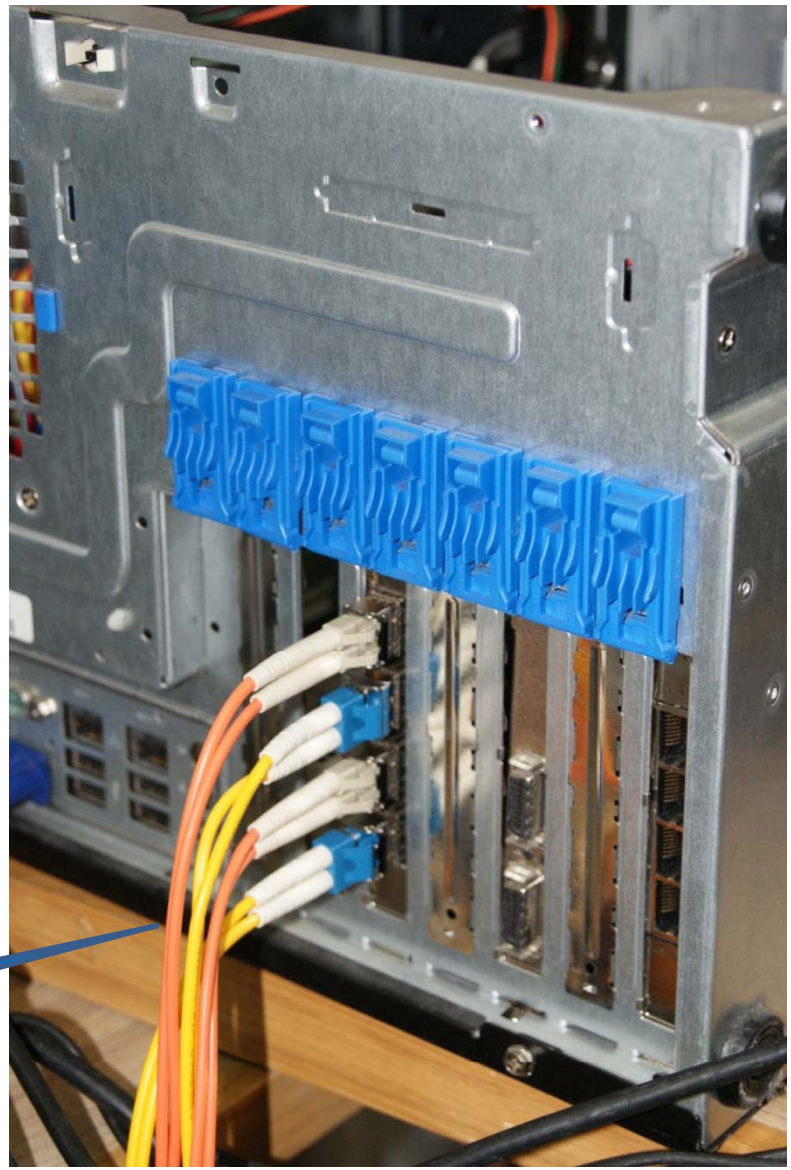
Multi-10G Network Analysis Solution



Installation View



Multi-10G Network Analysis System



4x10GE
Fiber Inputs

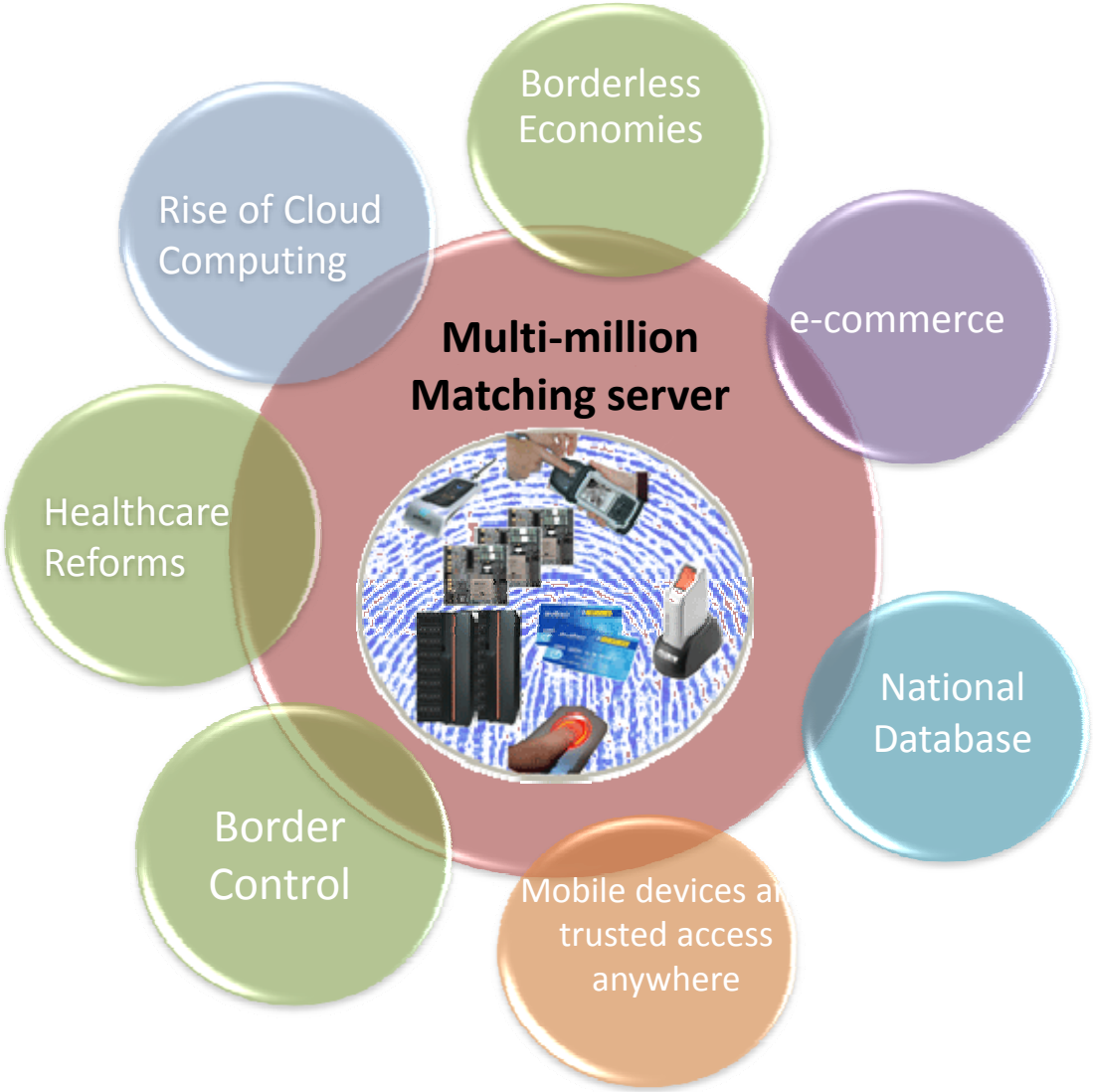
Multi-10G System in the network

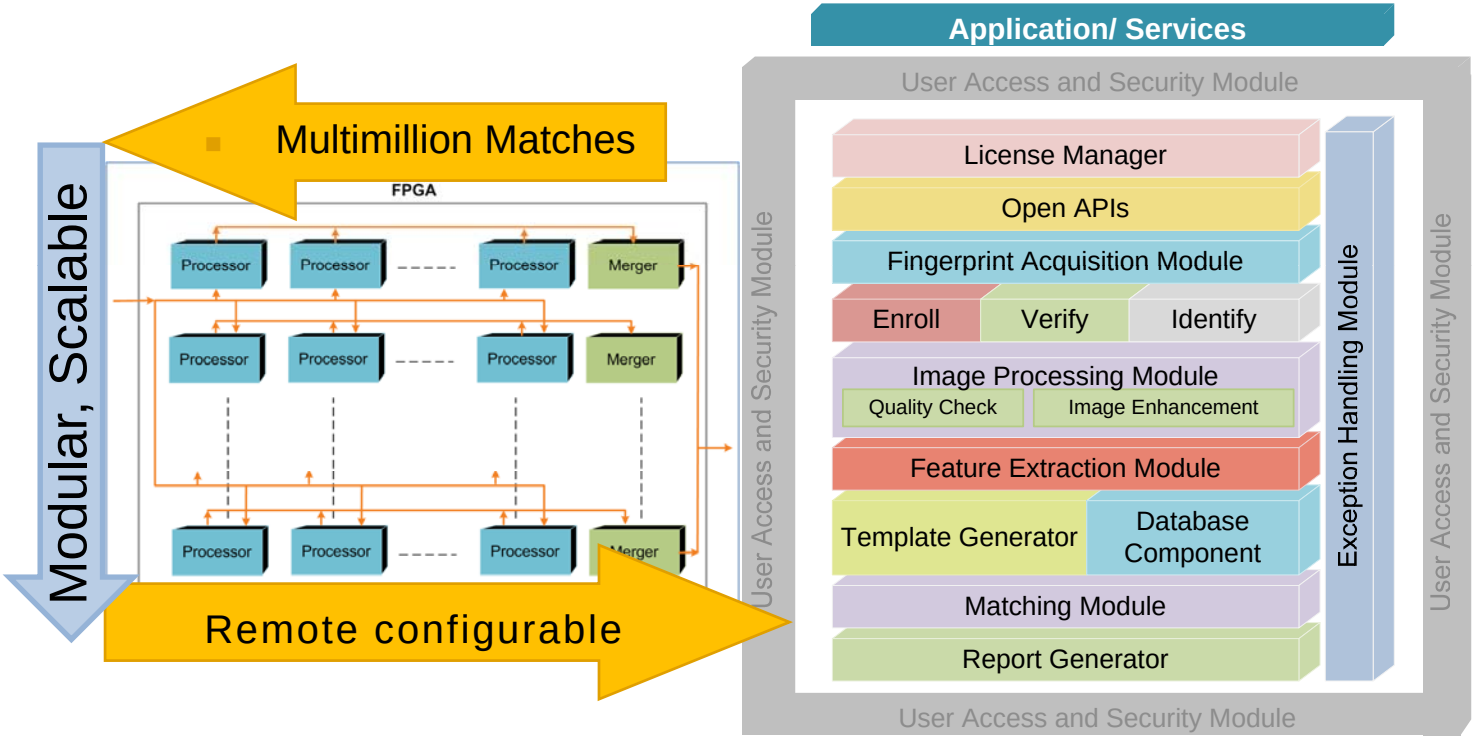
Design Examples

Massively Parallel Fingerprint Recognition System

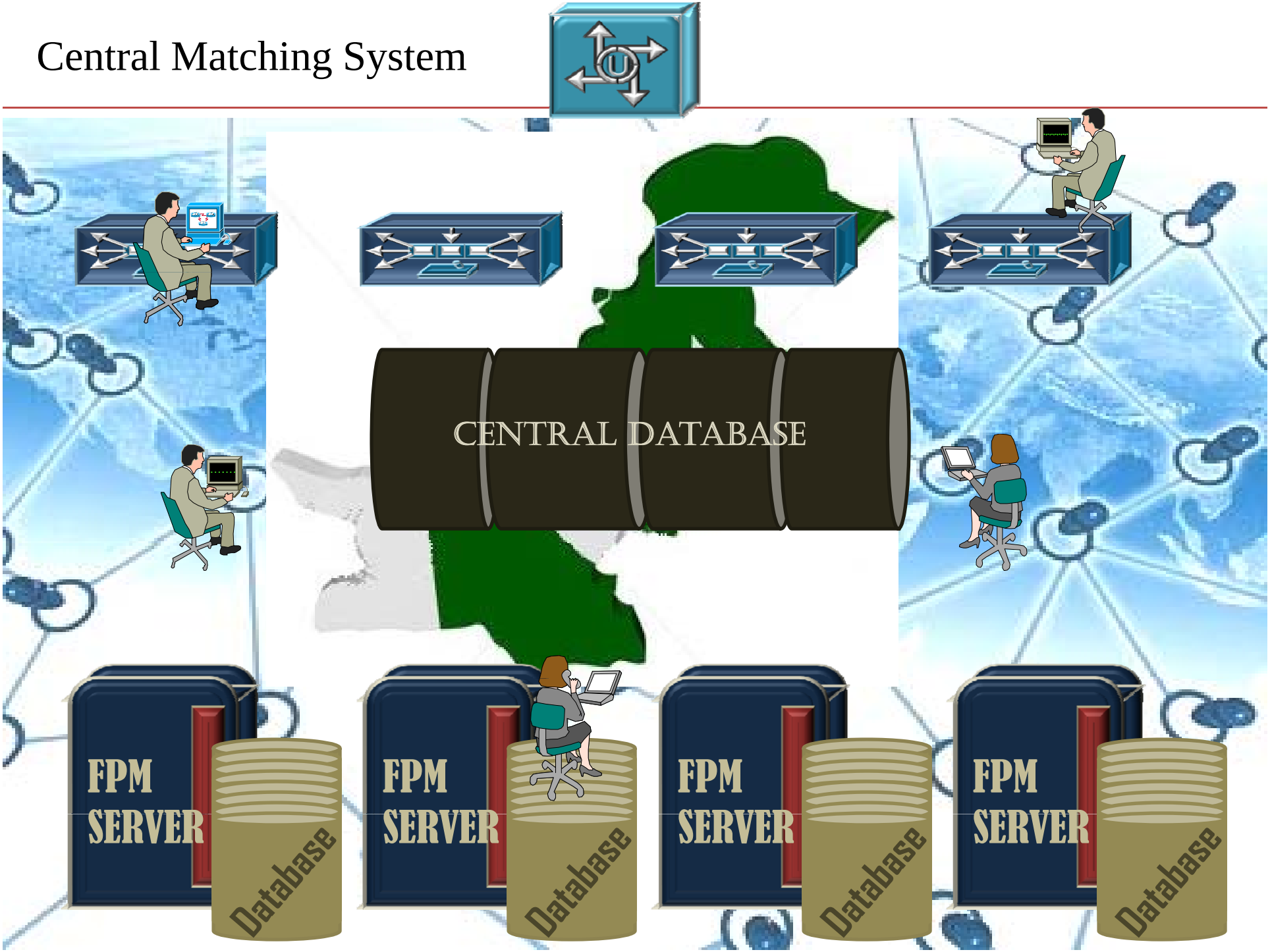
Massively Parallel Fingerprint Recognition System

- Real-time identity management of large user base requires a scalable massively parallel fingerprint recognition system




Application/ Services
User Access and Security Module
Multimillion Matches
FPGA
Processor
Merger
Modular, Scalable
Remote configurable
License Manager
Open APIs
Fingerprint Acquisition Module
Enroll
Verify
Identify
Image Processing Module
Quality Check
Image Enhancement
Feature Extraction Module
Template Generator
Database Component
Matching Module
Report Generator
Exception Handling Module
User Access and Security Module
User Access and Security Module
User Access and Security Module

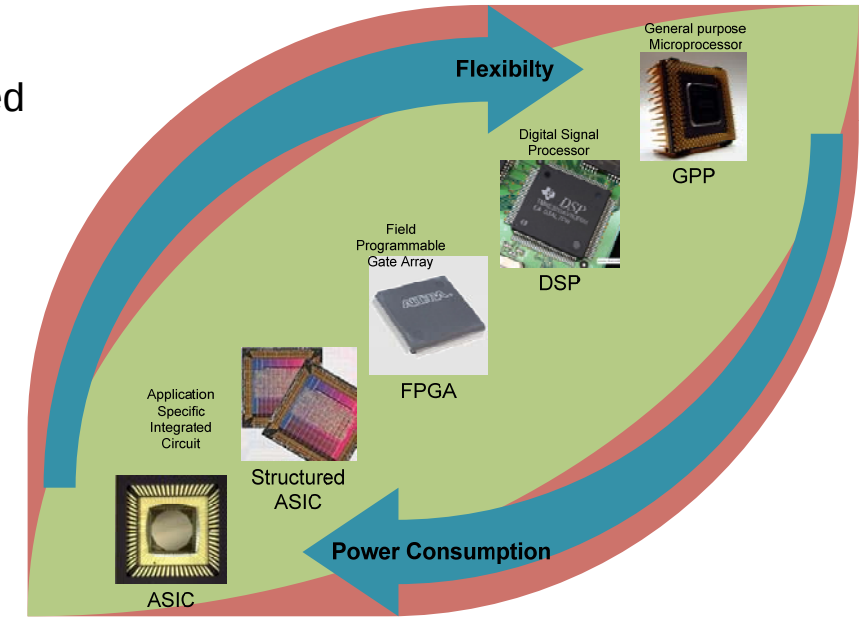
Central Matching System



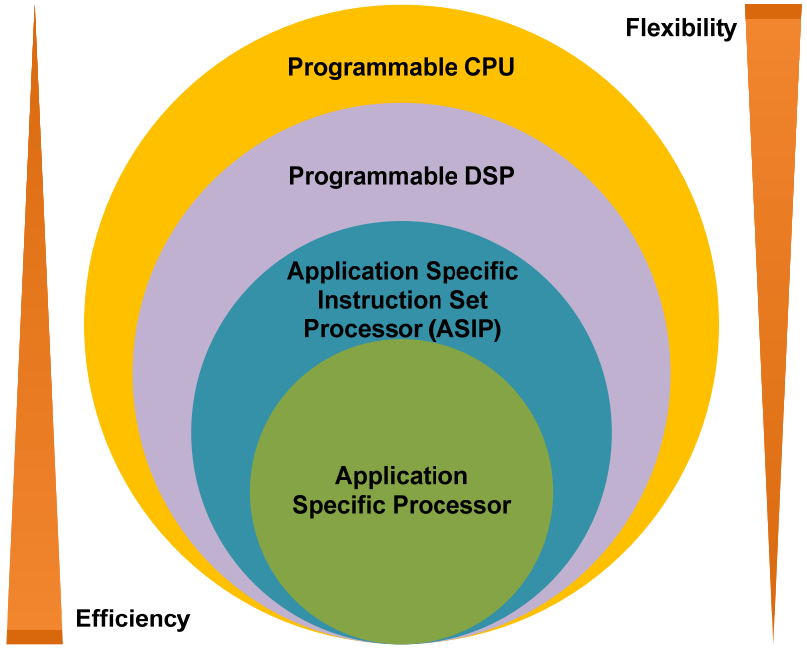
Extension of application as global authentication service

Design Strategies

- GPP
  - programming flexibility
  - High code and low computationally intensive code mapping
  - High power consumption
- DSP
  - Programming flexibility
  - Computationally intensive & Non structured code
- FPGA
  - Computationally intensive structured code
  - Programmability is more complex
- ASIC
  - Lower cost, low power
  - No flexibility of programming
  - Standard algorithms



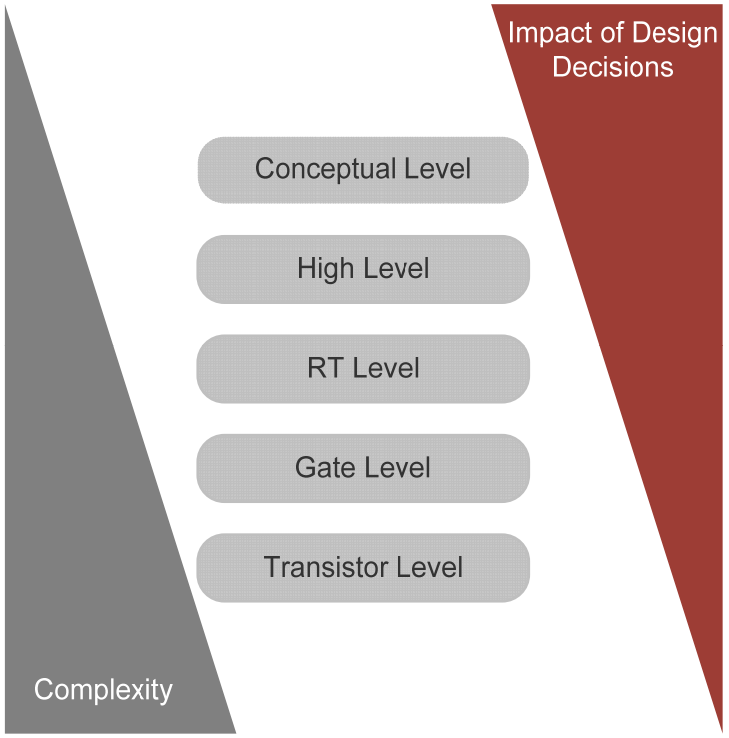
Flexibility vs Efficiency



- Efficiency verses flexibility tradeoff goes up
  - GPP
  - DSP Application Specific solution
  - HW based Instruction set of dedicated design on an FPGA or ASIC

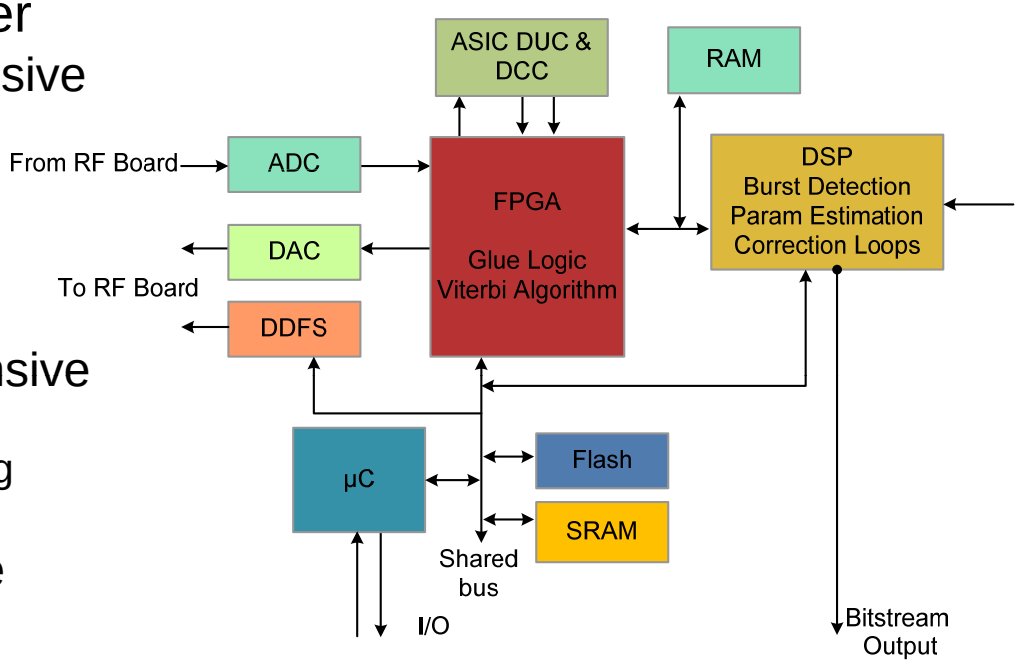
Design decision and complexity

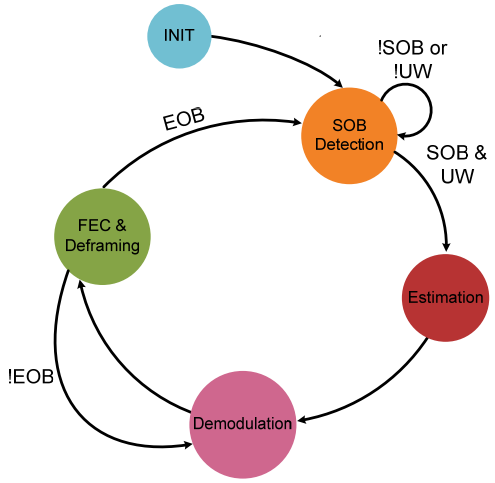
- Conceptual level design decisions are less complex but have a grave impact on the design
- The complexity increases as design moves down in the design cycle
- High level design decisions are very critical



Example: Design Partitioning and Mapping

- A Satellite burst modem receiver
  - DSP maps irregular code intensive application
    - Burst detection
    - Parameter Estimation
    - Correction loops
    - Demodulation
  - FPGA maps regular code intensive and interfaces
    - Forward Error Correction Coding
    - Glue Logic
  - ASICs standard code intensive
    - Digital Down Converter
  - GPP maps code intensive and user interfaces
    - Modem control software
    - Initialization and configuration software
    - User interface





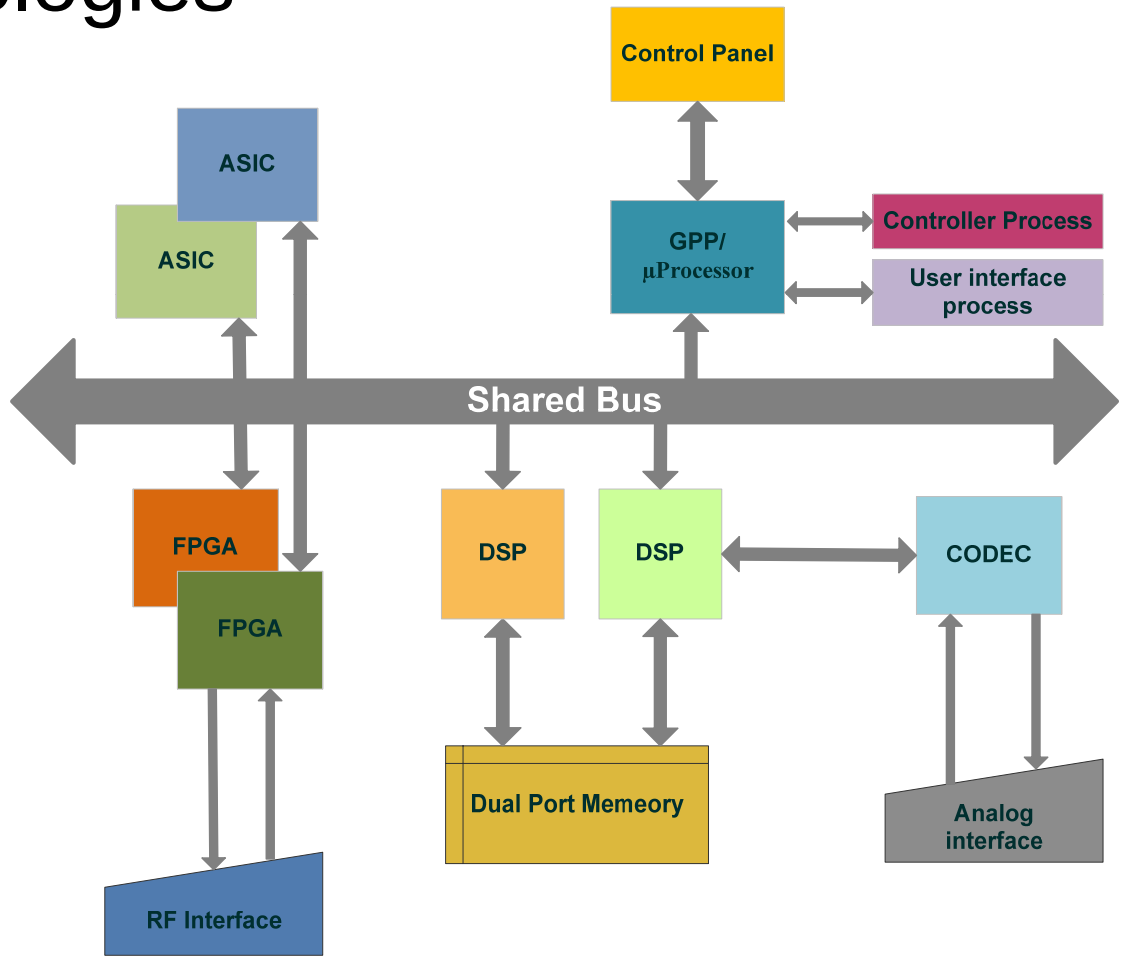
Design Examples

Software Defined Radios

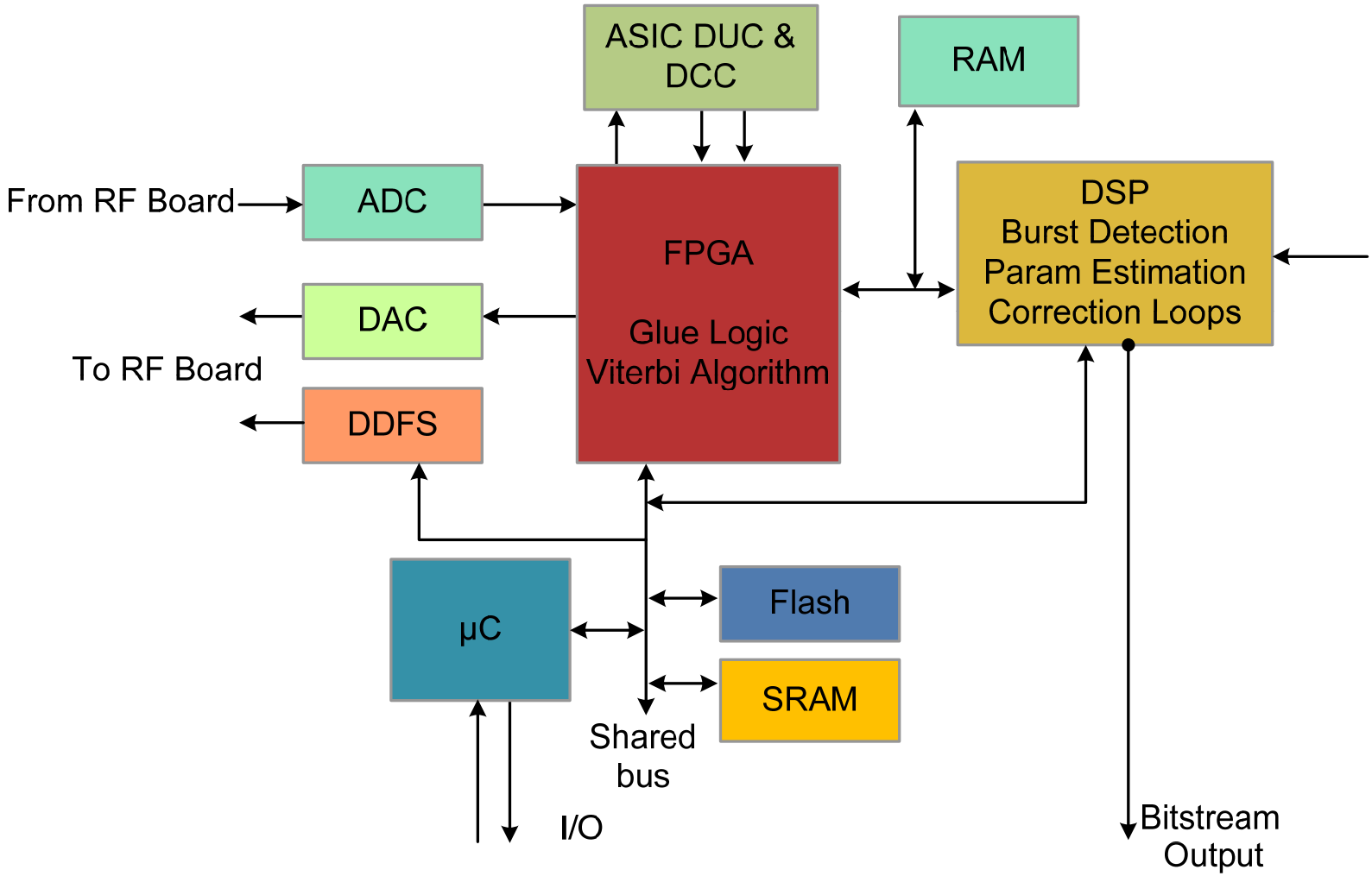
Indigenously Developed SDR

A Typical Digital System

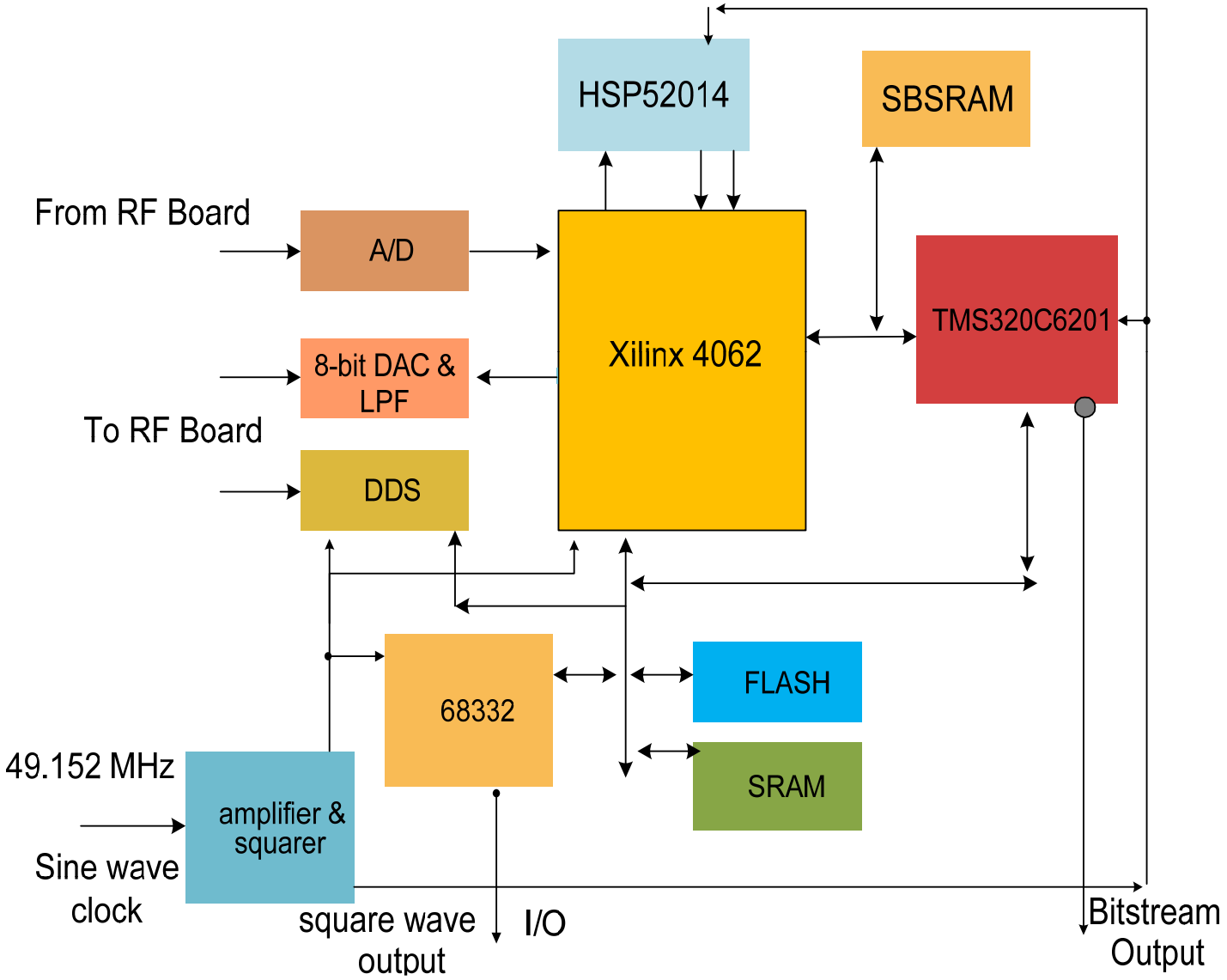
- Hybrid technologies
  - ASICs
  - DSPs
  - FPGAs
  - Interfaces



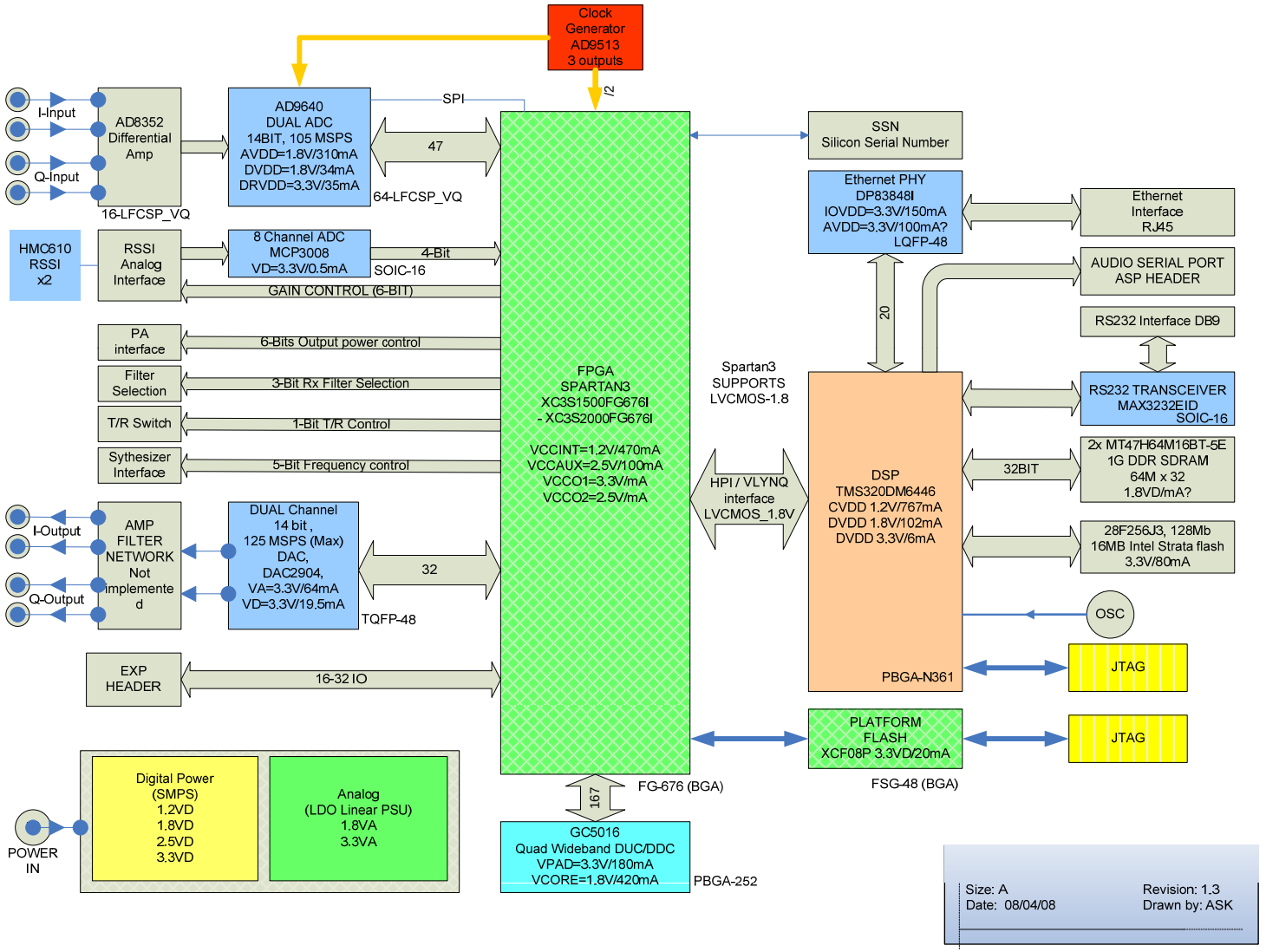
Design Partitioning and Mapping



Example Embedded System Satellite Burst Receiver: 1997-98

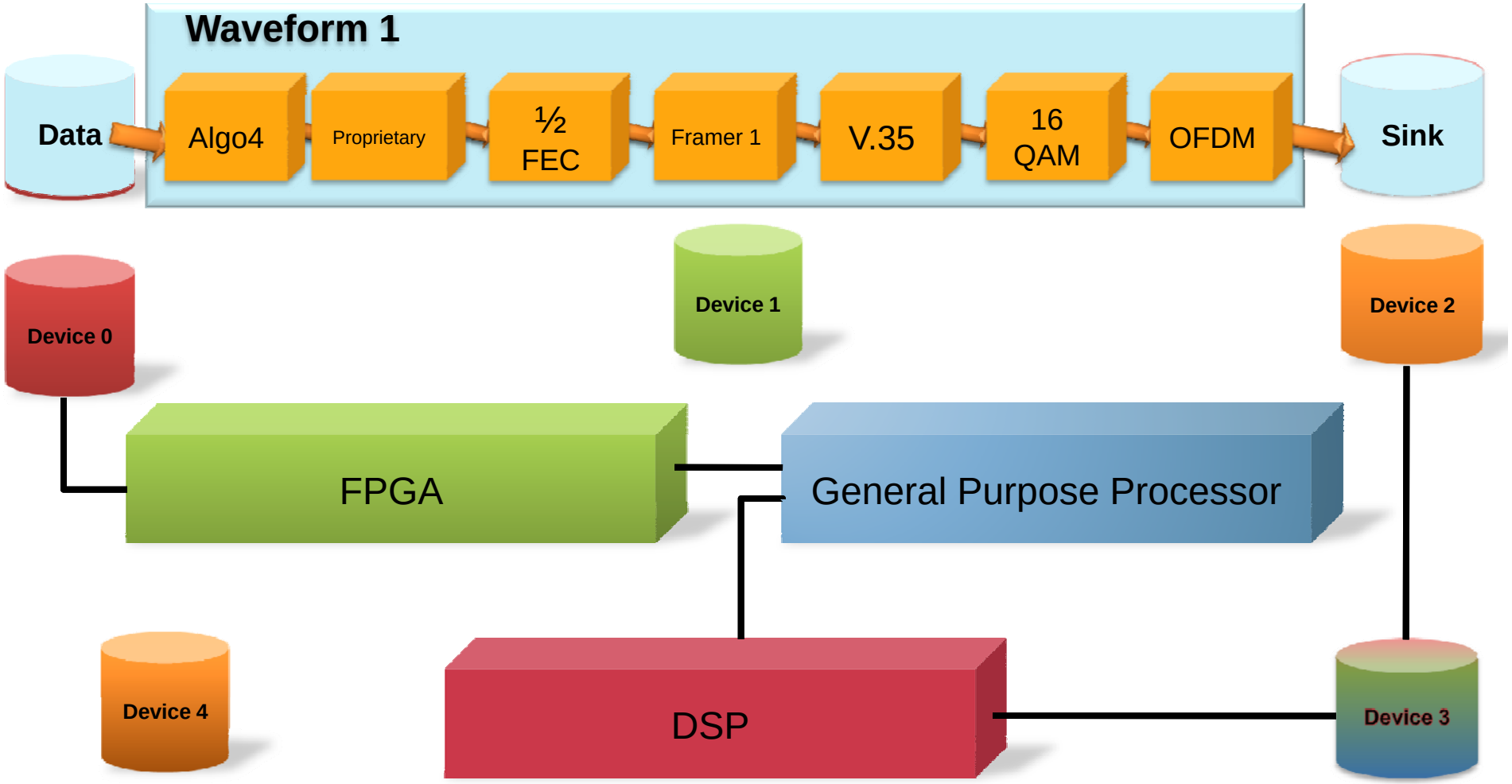


SDR Design 2010



Software Defined Radio

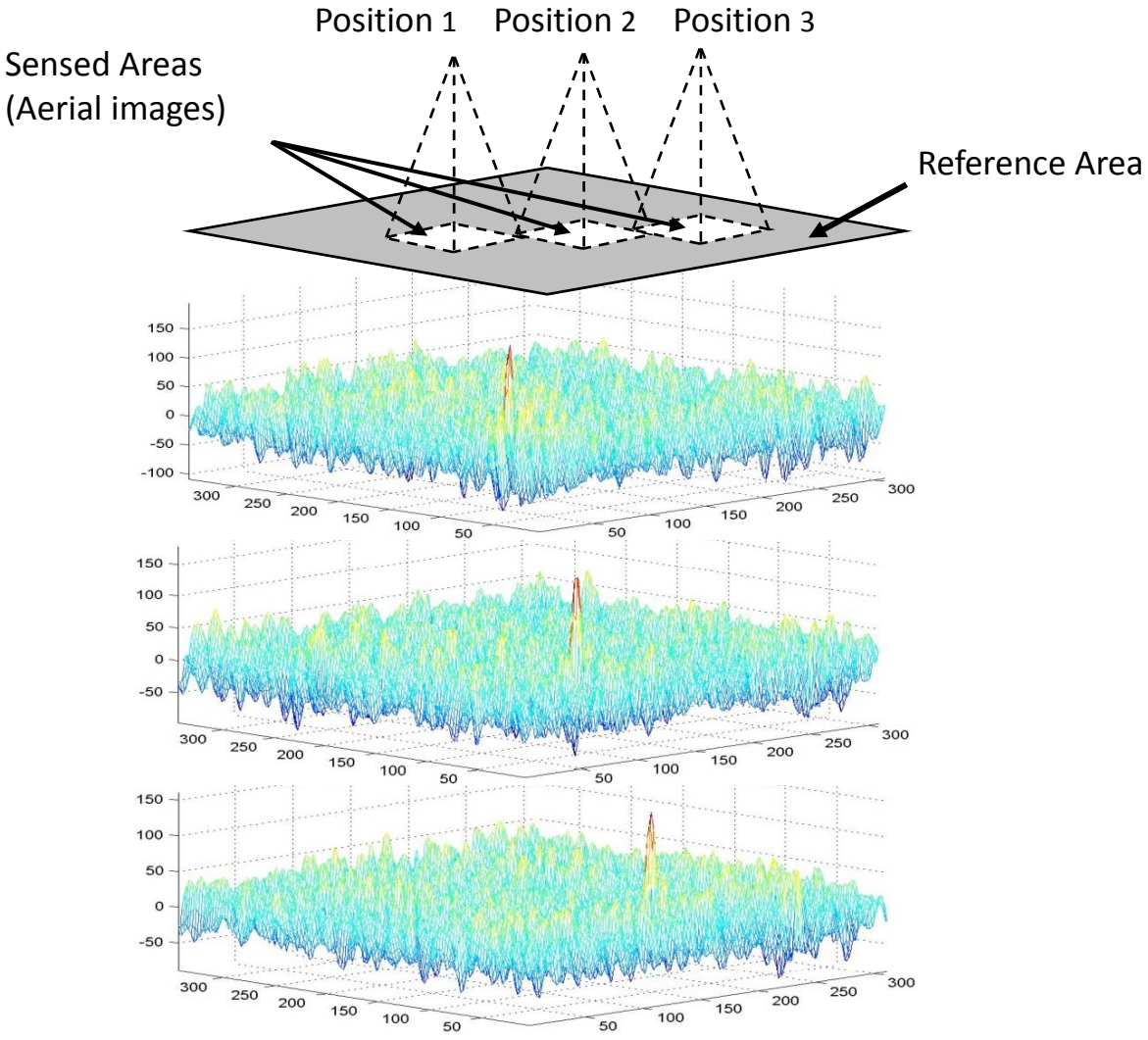
All configurable HW



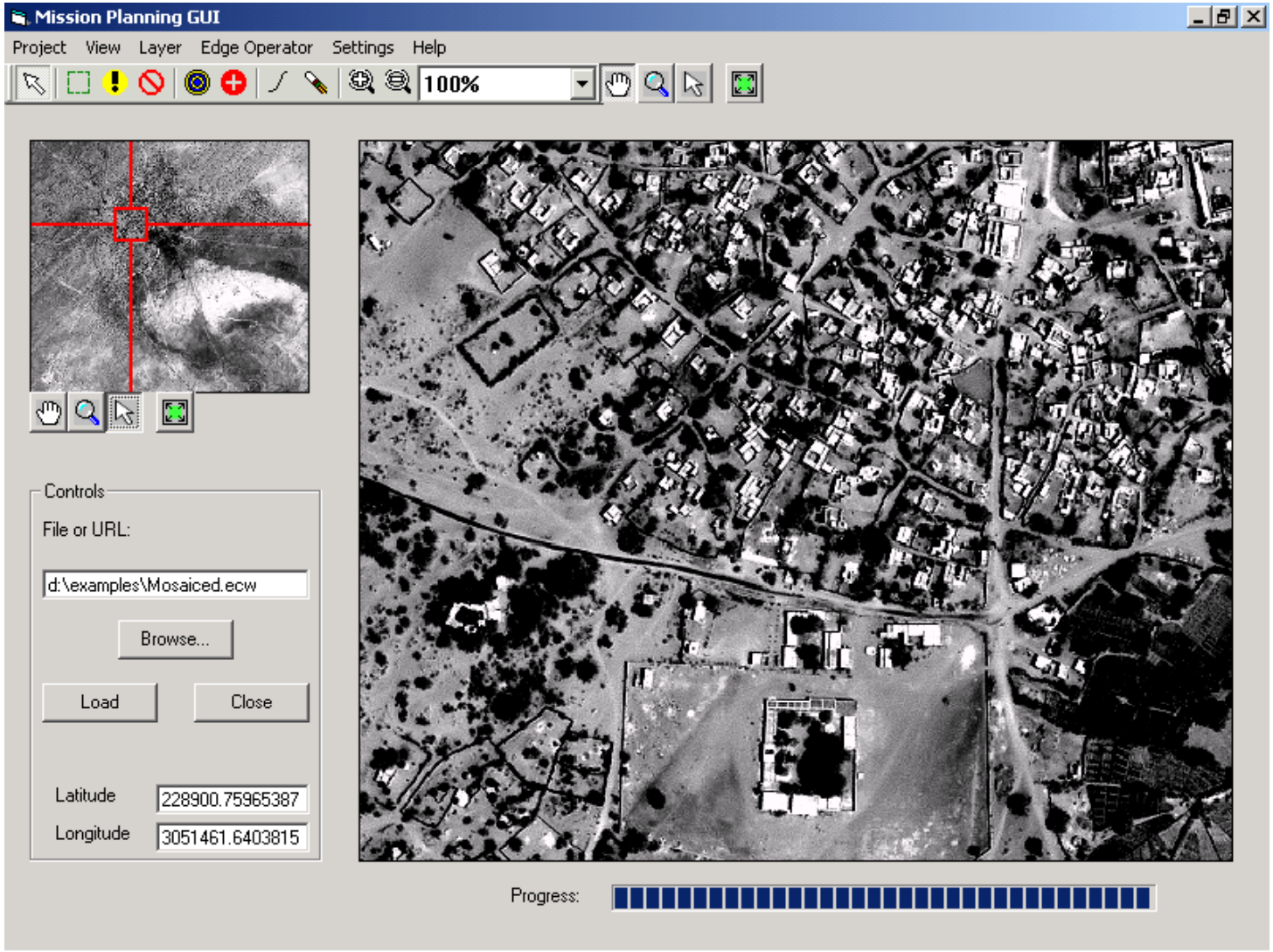
Design Examples

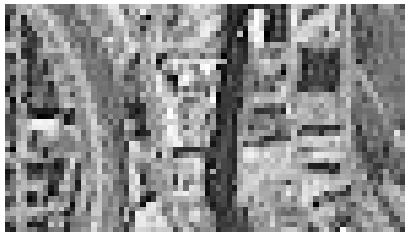
Passive Navigation System

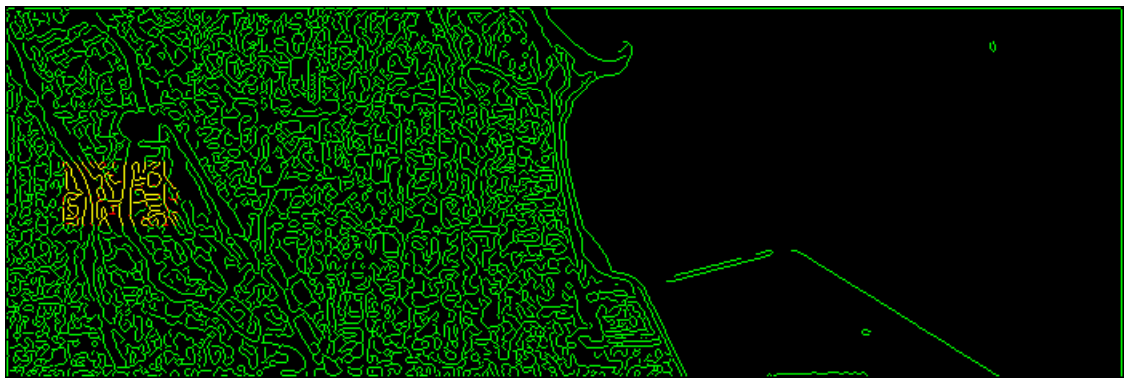
Working of the System



Working

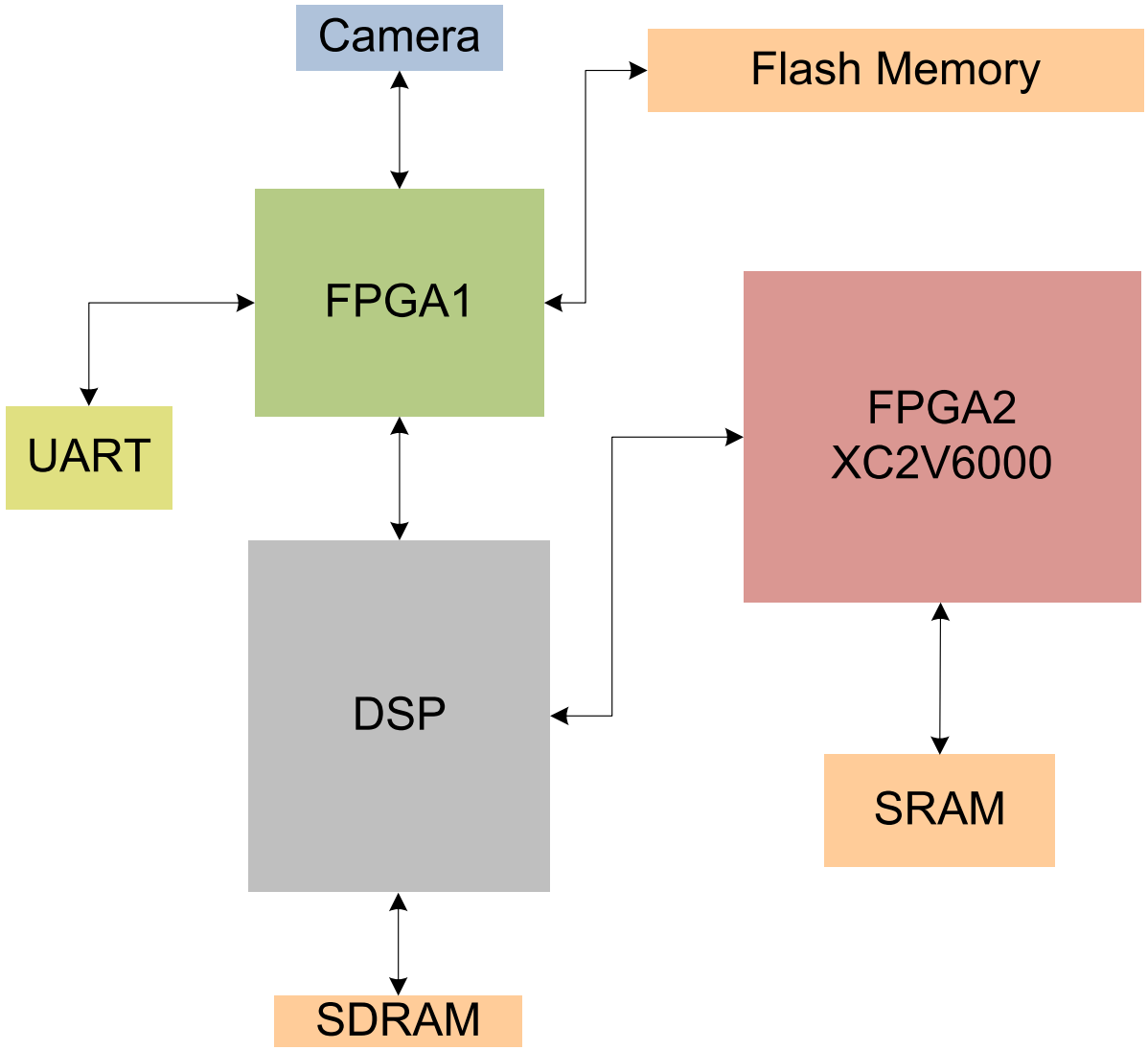

Mission Planning GUI
Project View Layer Edge Operator Settings Help
100%
Controls
File or URL:
d:\examples\Mosaiced.ecw
Browse...
Load
Close
Latitude
228900.75965387
Longitude
3051461.6403815
Progress:



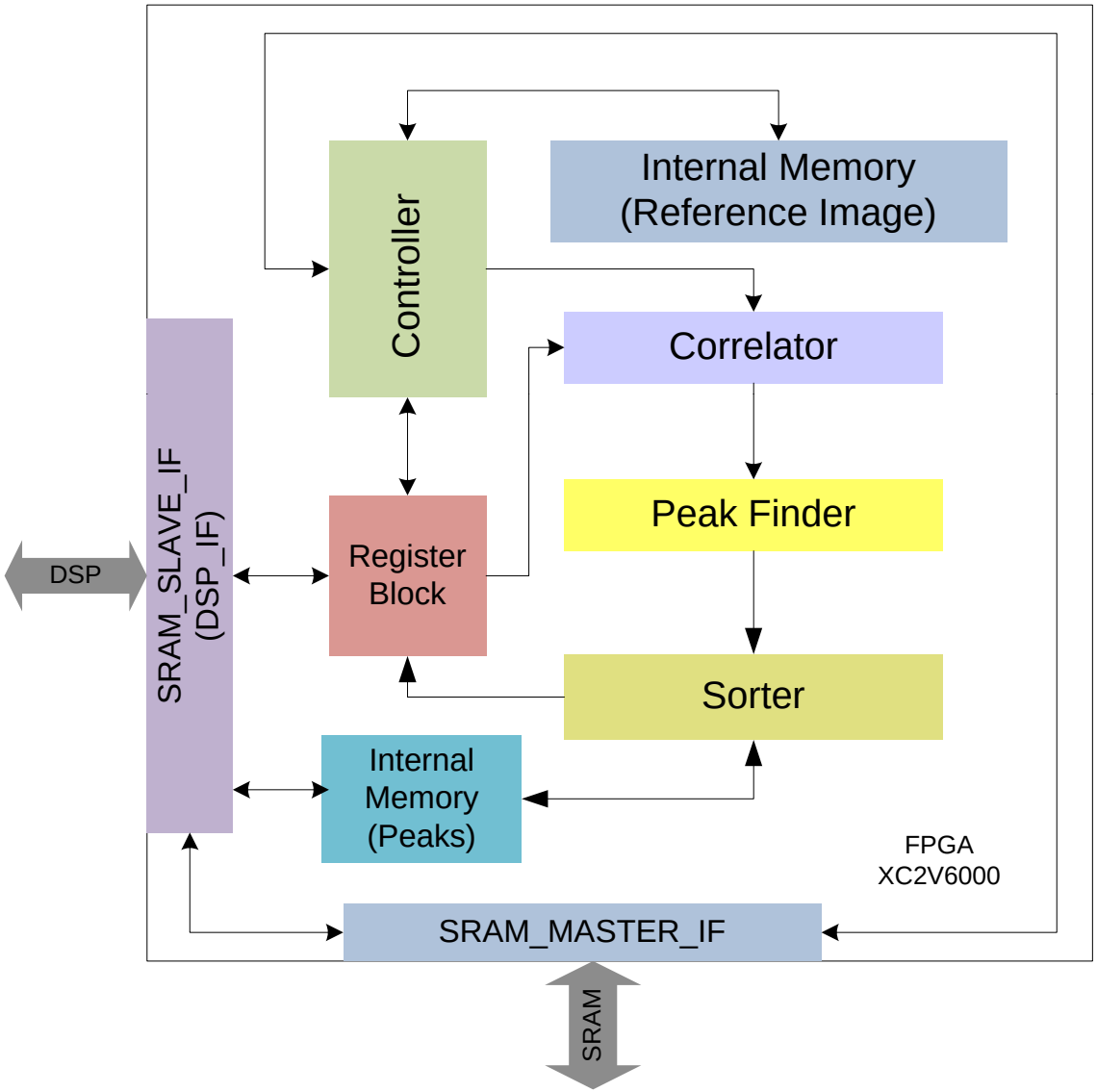


Passive Navigation System (in Production)

Embedded Solution



FPGA2

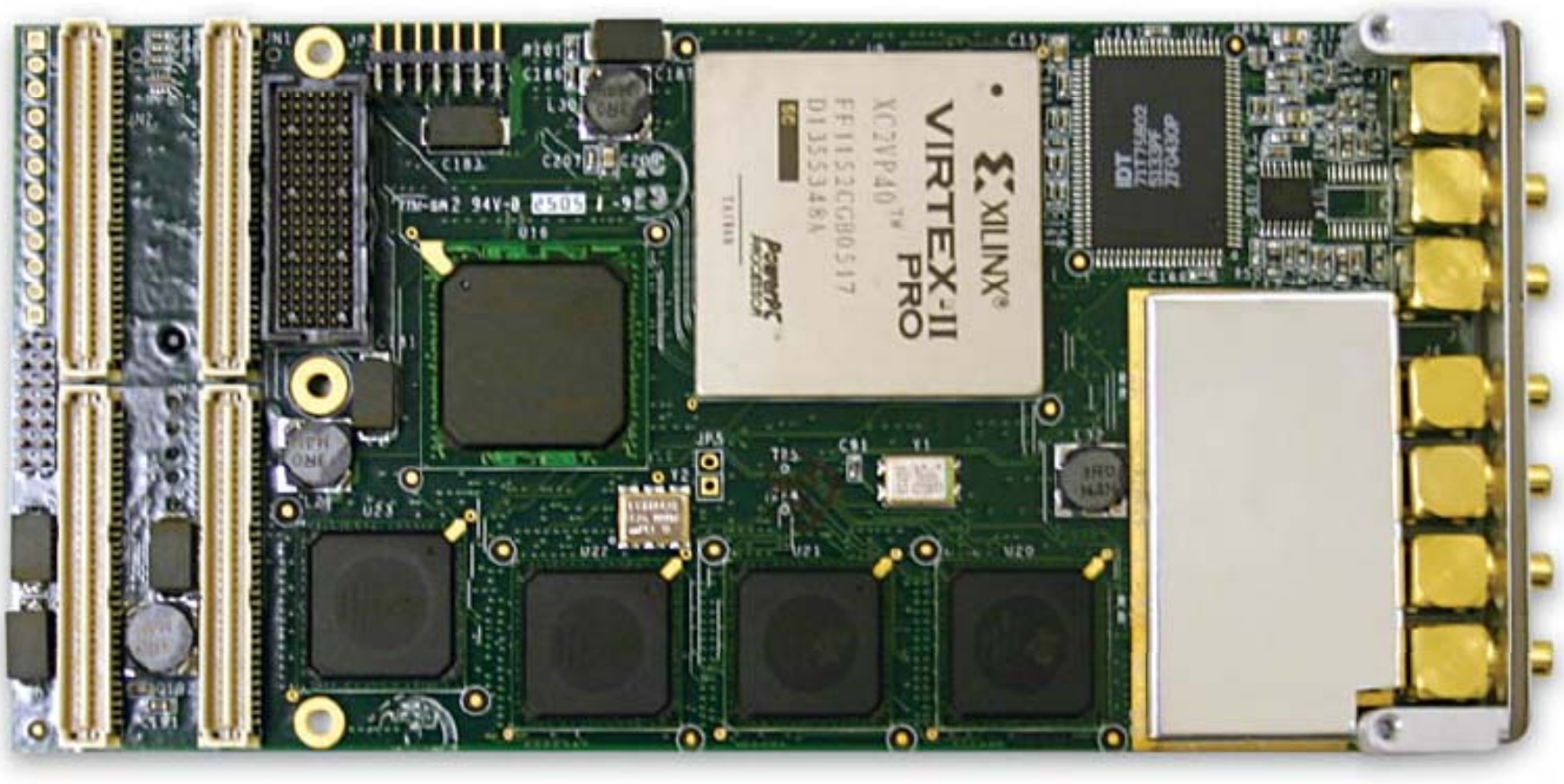

Controller
Internal Memory
(Reference Image)
Correlator
Peak Finder
Sorter
SRAM_SLAVE_IF
(DSP_IF)
DSP
Register
Block
Internal
Memory
(Peaks)
FPGA
XC2V6000
SRAM_MASTER_IF
SRAM

Design Examples

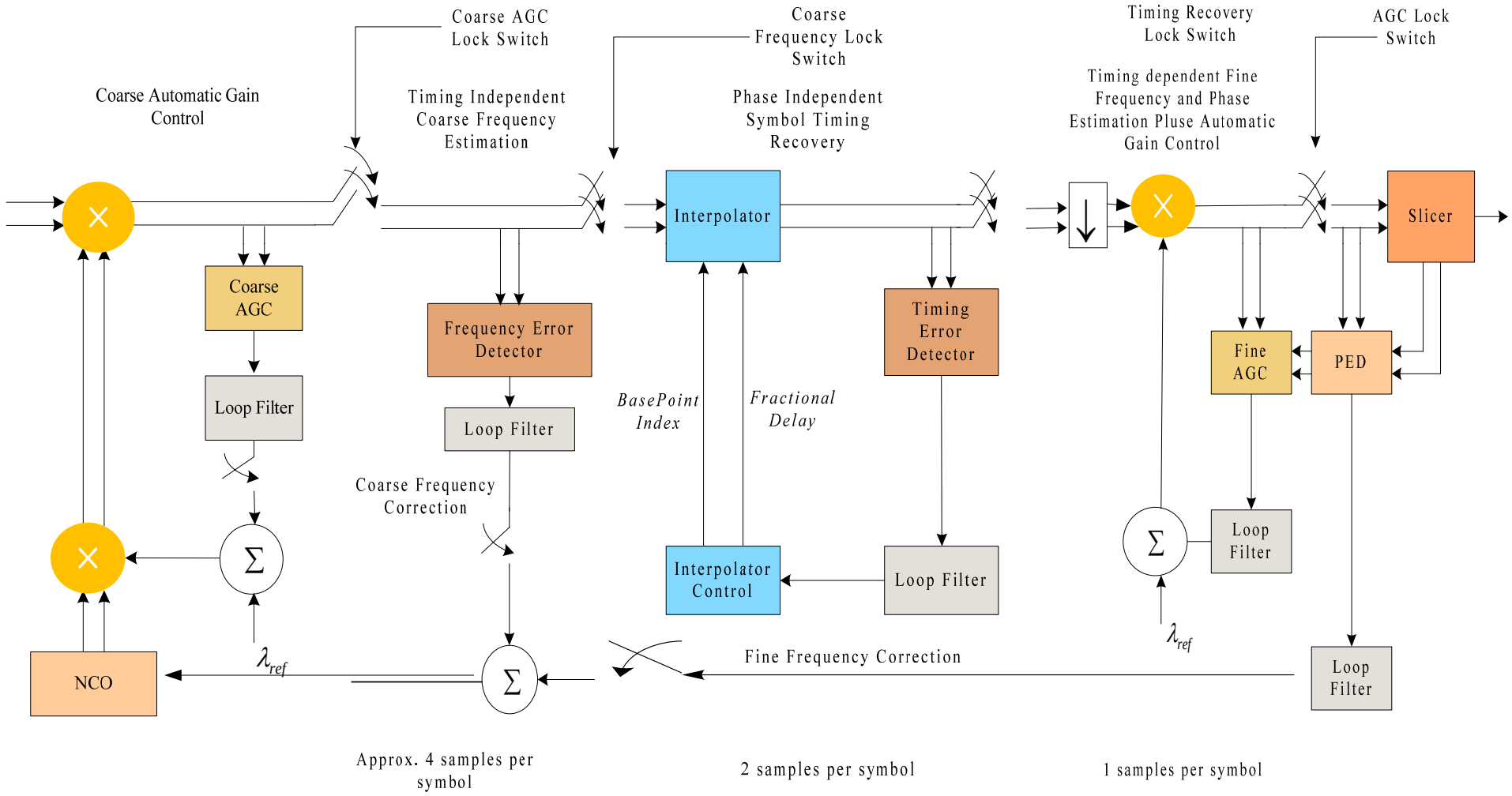
Spectrum Monitoring System

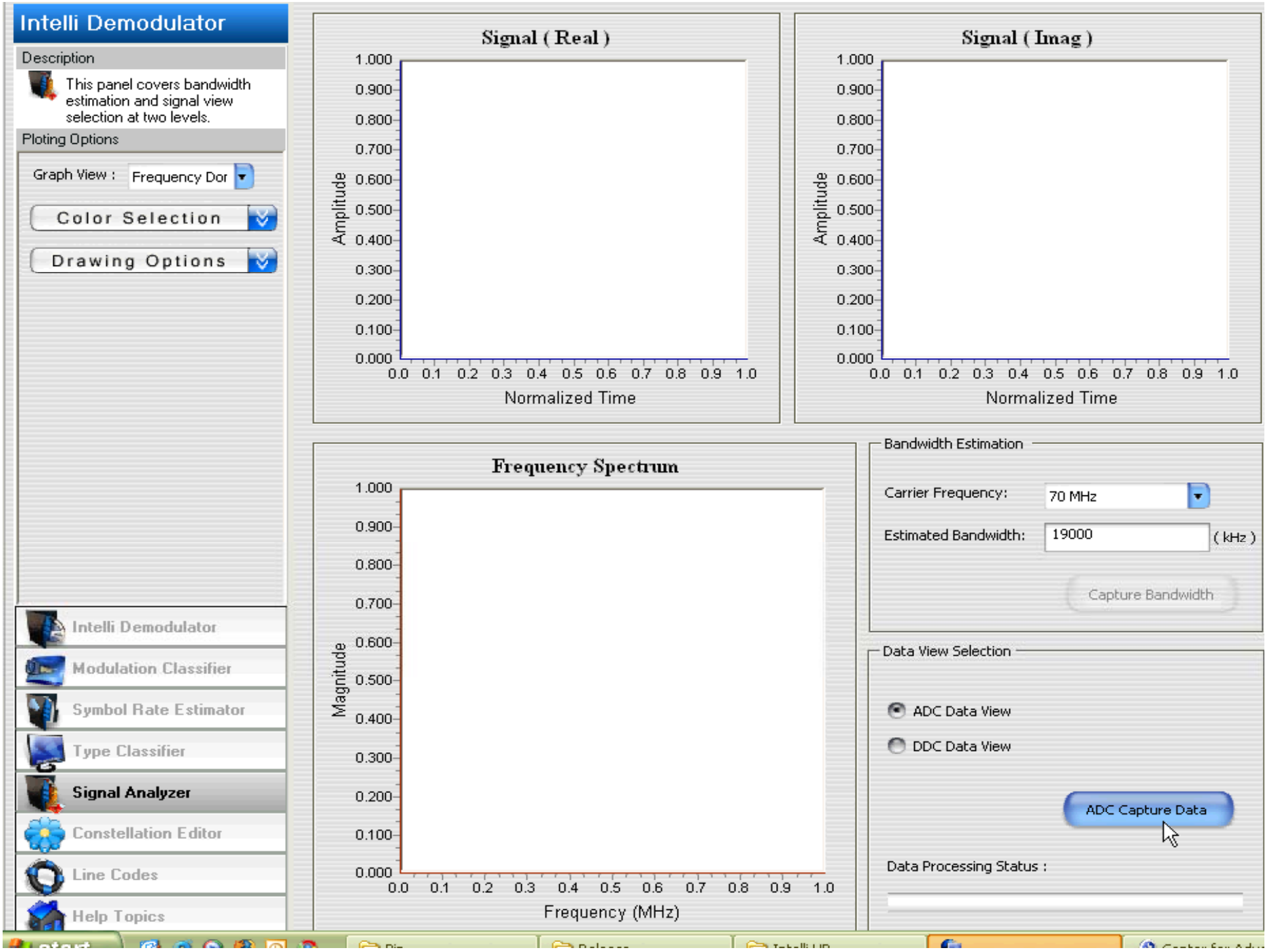
Spectrum Analysis System

Hardware Multiple Boards



Universal Demodulator Design




Intelli Demodulator
Description
This panel covers bandwidth estimation and signal view selection at two levels.
Ploting Options
Graph View :
Frequency Dor
Color Selection
Drawing Options
Intelli Demodulator
Modulation Classifier
Symbol Rate Estimator
Type Classifier
Signal Analyzer
Constellation Editor
Line Codes
Help Topics
Signal (Real)
Amplitude
Normalized Time
Signal (Imag)
Amplitude
Normalized Time
Frequency Spectrum
Magnitude
Frequency (MHz)
Bandwidth Estimation
Carrier Frequency:
70 MHz
Estimated Bandwidth:
19000
(kHz)
Capture Bandwidth
Data View Selection
ADC Data View
DDC Data View
ADC Capture Data
Data Processing Status :

Summary

- Advancement in VLSI technology has enabled engineers to develop products and solutions to complex engineering problems
- Digital designs are fun to exercise
- The algorithms are mapped using digital design techniques that exploit multi layers of parallelism
- The FPGA technology is very handy and can be put to use for devising innovative solutions

Grading

- Quizzes 5% ,
- Labs & assignments to be developed ALONE: 10-15%,
- Final project, teams of 1-3 students: 10-15%,
- One/Two sessionals: 25-30%,
- Final: 35-50