DIGITAL SYSTEM DESIGN

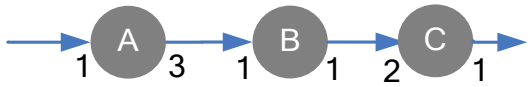
SESSIONAL EXAM
SAMPLE PAPER

Time: 1 Hrs
Marks: 50

1.1 Question: Flow Graph Synthesis

The following Flow Graph shows a multi rate DFG.

a. Design a sequential HW realization of the graph showing all the Multiplexer, De-multiplexer, registers and clocks in the design.
b. Write RTL Verilog code to implement the design in HW.
c. Write Balanced Equations for the graph and solve the equations to find a parallel HW realization of the design. Draw the realization.



6,7,7

1.2 Question: Digital Design with Compression Tree

a. Add two fixed-point signed numbers, give the equivalent floating point value of the operand and the sum,
   a = 111_10 in Q3.2 and
   b = 000111_011 in Q6.3 format
b. Perform signed by signed multiplication of the numbers given in part a, give equivalent floating point value of the product

5,5

1.3 Question: Fixed-point Conversion

Convert the following C code to **its equivalent fixed point listing in C.** Consider x,b,a, and out in Q1.15 format and acc in Q8.32 format. Check corner cases and saturate the result if overflow occurs.

```
float recursion_float (float x[], float y[], float b[], float a[])
{
      float acc, out;
      int i;
      acc = 0;
      for( i = 0; i < 2; i++)
      {
            acc += b[i] * x[i] + a[i] * y[i];
      }
      out=acc;
return out;
}
```

The constants are

```
float b[] = {0.258, -0.309, -0.704};
float a[] = {-0.123, -0.51, 0.223};
float x[] = {-0.19813, -0.76291,0.57407);
float y[] = {0.123, -0.213, -0.912}
```

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