Assignment # 1
EC-423 Digital System Design

Submission: 24 Sep 2012
Demonstrate in Lab

Assignment Objectives

In this assignment, you will learn the following

1. What are combinational circuits
2. Design of combinational circuits using K-maps
3. Design using Verilog

Combinational Circuits

Logic circuit can be classified into two types: Combinational and Sequential. The Combinational circuit consists of logic gates whose outputs are determined by the values of the inputs only. The output is computed using logic operations.

Design procedure

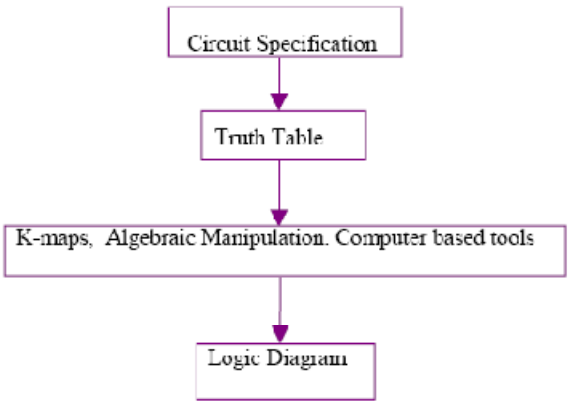

Figure 1: Flow of Logic Design

Problem Statement: BCD to 7-segment display controller

Design a BCD to seven-segment decoder, first using K-Maps and then coding the logic using high level Verilog description. Instantiate both modules in a top-level stimulus and test it for different input signals.

Background

As we know 0 to 9 digits can be displayed using seven Light emitting diode segments (or LED's) arranged to look like digit 8 as shown in figure. By controlling which segment is ON and which is OFF we can display illuminated patterns that correspond to the 10 decimal digits 0 to 9 as shown in Figure 2.

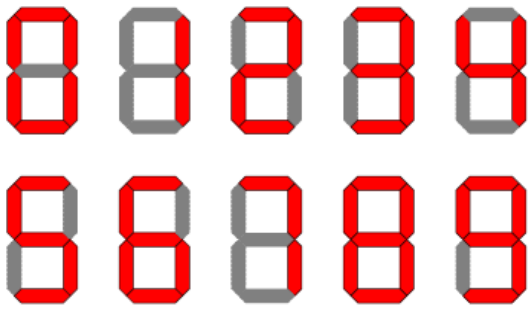

Figure 2: Patterns for generating 0-9 numbers using 7 LEDs segments

The objective of the assignment is to design two modules in Verilog those will take a BCD number as input, and produce the control signals C0 to C6 at the output. These outputs allow illuminating the corresponding segments in the 7-segment display.

1. For the first method, generate a truth table, use k-Map for optimization of the logic. By using assign statement in Verilog implements the optimized logic.
2. For the second module, use high level Verilog construct and develop the same logic that implements the design.

Test your logic using a stimulus.

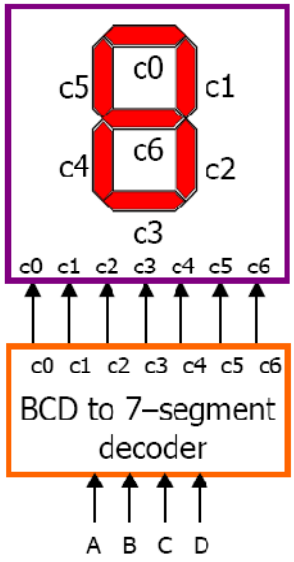

Figure 3: inputs and outputs for BCD to 7-segment display