

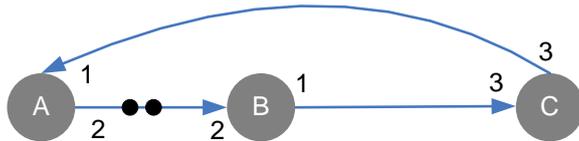
ADV DIGITAL SYSTEM DESIGN
SESSIONAL II
SAMPLE EXAM

Time: 1 Hrs

Marks: 50, (10)

1.1 Question: Flow Graph Synthesis

Write Balanced Equations for the graph and solve the equations to find a parallel HW realization of the design. Draw the realization.



7,8

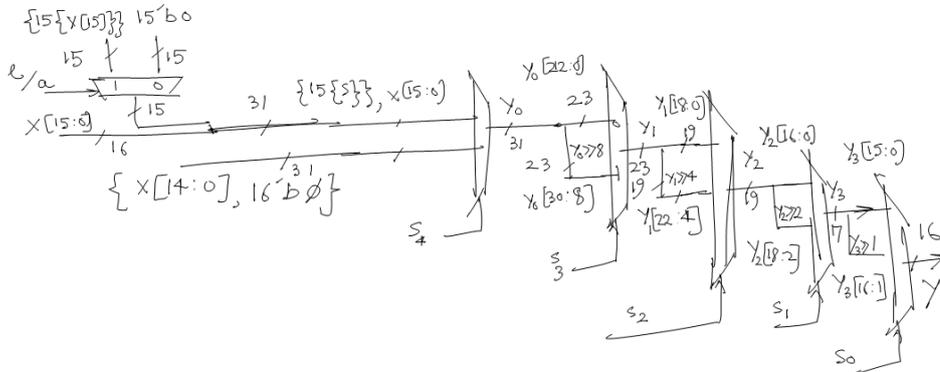
1.2 Question: Digital Design with Adders

- Add the following numbers using Carry Skip Adder, clearly shows how logic helps in quick computation of carry, break the number in block of 3-bits each
 $a = 111_101_011_110$
 $b = 011_010_100_100$
- Design an optimal architecture of a Conditional Sum Adder to add two Q-format numbers a and b in Q1.5 and Q3.4 formats respectively. Add $a = 1_01110$ and $b = 101_1010$ using Conditional Sum Adder.
- Reduce the multi operand expression using Dadda Reduction Scheme by first representing each bit as a dot and then compression them using the scheme.
 $y = a + b + c + d + e + f + g$
 Where a, b, c, d, e, f and g are in Q1.2, Q1.3, Q1.4, Q1.3, Q1.5, Q2.1, Q3.1 formats respectively.

6,7,7

1.3 Question: Barrel Shifter (Take Home)

Write RTL Verilog Code for the design of a 4-stage pipeline hierarchical Barrel shifter. This requires adding 4-pipeline registers in the following figure. (Copy the code in a separate sheet to verify the design for a number of inputs as a take home part of the exam. SUMBIT your code in next Tuesday Class)



15, (10)